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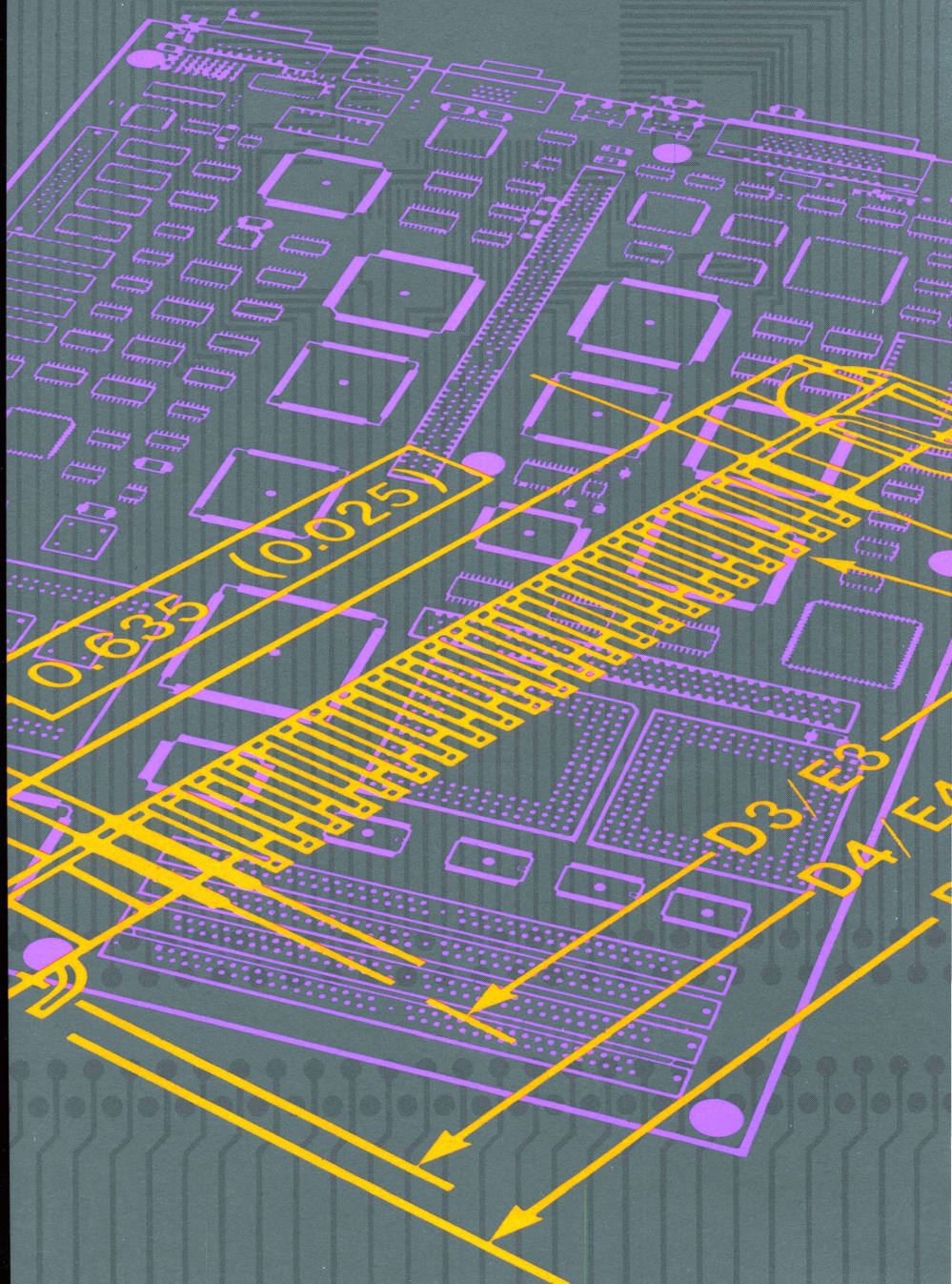

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PACKAGING HANDBOOK

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IC Assembly Technology 3

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Introduction 1

CHAPTER 1
INTRODUCTION

OVERVIEW OF INTEL PACKAGING TECHNOLOGY

As semiconductor devices become significantly more complex, electronics designers are challenged to fully harness their computing power. Today's products can feature more than three million transistors, and device count is expected to increase to one hundred million by the year 2000. With a greater number of functions integrated on a die or chip of silicon, manufacturers and users will face new and increasingly challenging electrical interconnect issues. To tap the power of the die efficiently, each level of electrical interconnect from the die to the functional hardware or equipment must also keep pace with these revolutionary devices. Package design, at the first interconnect level, has a major impact on device performance and functionality.

Today, submicron feature size at the die level is driving package feature size down to the design-rule level of the early transistors. At the same time, electronic equipment designers are shrinking their products, increasing complexity, and setting higher expectations for performance. To meet these demands, package technology must deliver higher lead counts, reduced pitch, minimum footprint area, and significant overall volume reduction.

Circuit performance is only as good as the weakest link. Therefore, device performance is for all practical purposes determined by the package. While packaging cannot add to the theoretical performance of the device design, it can have adverse effects if not optimized. An optimum package design would achieve 100% of the theoretical device, application-specific performance, which in practice is un-achievable. Package performance, therefore, is the best compromise of electrical, thermal, and mechanical attributes, as well as physical outline, to meet product specific reliability and cost objectives.

These factors have driven a variety of major innovations in Intel package design, such as surface mount, small out-line, and very thin packages. The introduction of additional advanced Intel packaging technologies to meet these evolving needs will continue aggressively throughout the 1990s. Intel introduced the multilayer molded plastic quad flatpack (MM-PQFP). The MM-PQFP, Intel's patented concept, enhances the electrical performance of the molded lead frame package by incorporating isolated ground and power planes within the assembly. After molding, the multilayer construction is totally embedded in the molded body which is not evident on the outside.

Fit, form, and function are in the eye of the beholder, and any Intel device can serve more than one market and/or application requiring widely divergent package attributes.

Therefore, "one size fits all" is not a practical approach to device packaging. Packaging technology is not a single technology, but instead consists of more than 20 industry proven combinations of technologies or technology sets that can be categorized by package families.

In support of the growing number of Intel devices and to meet the industry demand for package-specific applications, Intel's package portfolio has more than doubled during the last ten years.

PURPOSE OF THIS HANDBOOK

Intel's Packaging Handbook is intended to serve as a data reference for engineering design, as well as a guide to Intel package selection and availability. Each of the ten chapters provides a comprehensive and in-depth analysis of Intel packaging technology, from information on IC assembly, performance characteristics, and physical constants, to detailed discussions of surface mount technology and Intel shipping and packing.

Chapter 1 provides an analysis of Intel's package families, including package attributes, package types, and a package selection guide. (CD-ROM Literature Order Number: 240817-004)

Chapter 2 offers a detailed view into Intel package module outlines and dimensions. (CD-ROM Literature Order Number: 231369-010)

Chapter 3 covers assembly manufacturing technology. The chapter begins with a brief introduction and a discussion of statistical tools used in the manufacturing process. It also includes a comprehensive analysis of Intel's IC assembly process flow. (CD-ROM Literature Order Number: 240818-004)

Chapter 4 explores package characteristics and tabulates in-depth data of electrical, mechanical, and thermal IC package characteristics. (CD-ROM Literature Order Number: 240819-003)

Chapter 5 addresses physical constants of IC package materials. The charts in this chapter provide valuable information on mechanical, electrical, and thermal properties of case materials, lead/lead frames, and soldering material characteristics. (CD-ROM Literature Order Number: 240820-004)

Chapter 6 ESD/EOS precautions describes electrical static discharge and electrical over stress (CD-ROM Literature Order Number: 241422-002)

Chapter 7 explores surface mount technology. (CD-ROM Literature Order Number: 240821-004)

Chapter 8 describes Desiccant Packing Methods and Materials. Moisture Sensitivity and Package Cracking is also examined. (CD-ROM Literature Order Number: 241187-003)

Chapter 9 provides an in-depth analysis of Board Solder Reflow Process Recommendations. (CD-ROM Literature Order Number: 241188-003)

Chapter 10 describes the various packing and shipping methods used at Intel. Packing media, desiccant pack materials, and shipping data are clearly illustrated. (CD-ROM Literature Order Number: 240822-004)

Chapter 11 provides the reader with a listing of international packaging specifications and a comprehensive resource library. (CD-ROM Literature Order Number: 240829-002)

Appendix A1 provides dimensional data for Non-JEDEC EIAJ-style Trays used by Intel.

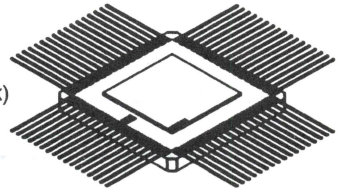
Glossary offers a detailed view of packaging related technical terminolgy. (CD-ROM Literature Order Number: 240823-004)

PACKAGE TYPES

CERAMIC PACKAGES

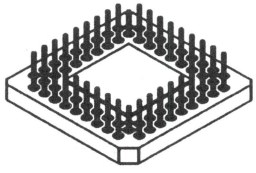
Surface Mount

CQFP
(Ceramic Quad Flatpack)



Socket Mount

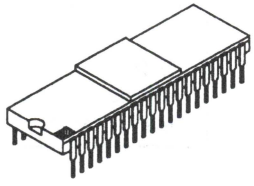
PGA
(Pin Grid Array)



(Bottom View)

Insertion/Socket Mount

C-DIP
(Ceramic Dual In-Line Package)
(Side-Braze)



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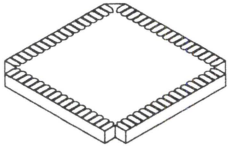
PACKAGE TYPES (Continued)

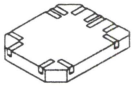
LEADLESS CHIP CARRIER PACKAGES

LCC
(Socket Mount)



(Bottom View)

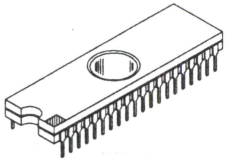
LCC
(Surface Mount)



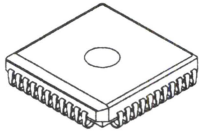
(Bottom View)

GLASS-SEALED PACKAGES

CERDIP
(Ceramic Dual In-Line Package)
(Insertion Mount; UV Window)

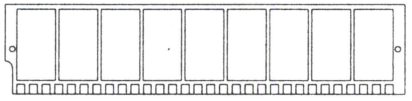


CERQUAD
(Ceramic Quadpack)
(Surface Mount)



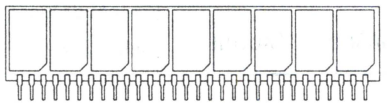
MODULES

SIMM
(Single In-Line Leadless
Memory Module)



(Top View)

SIP
(Single In-Line Leaded
Memory Module)



(Top View)

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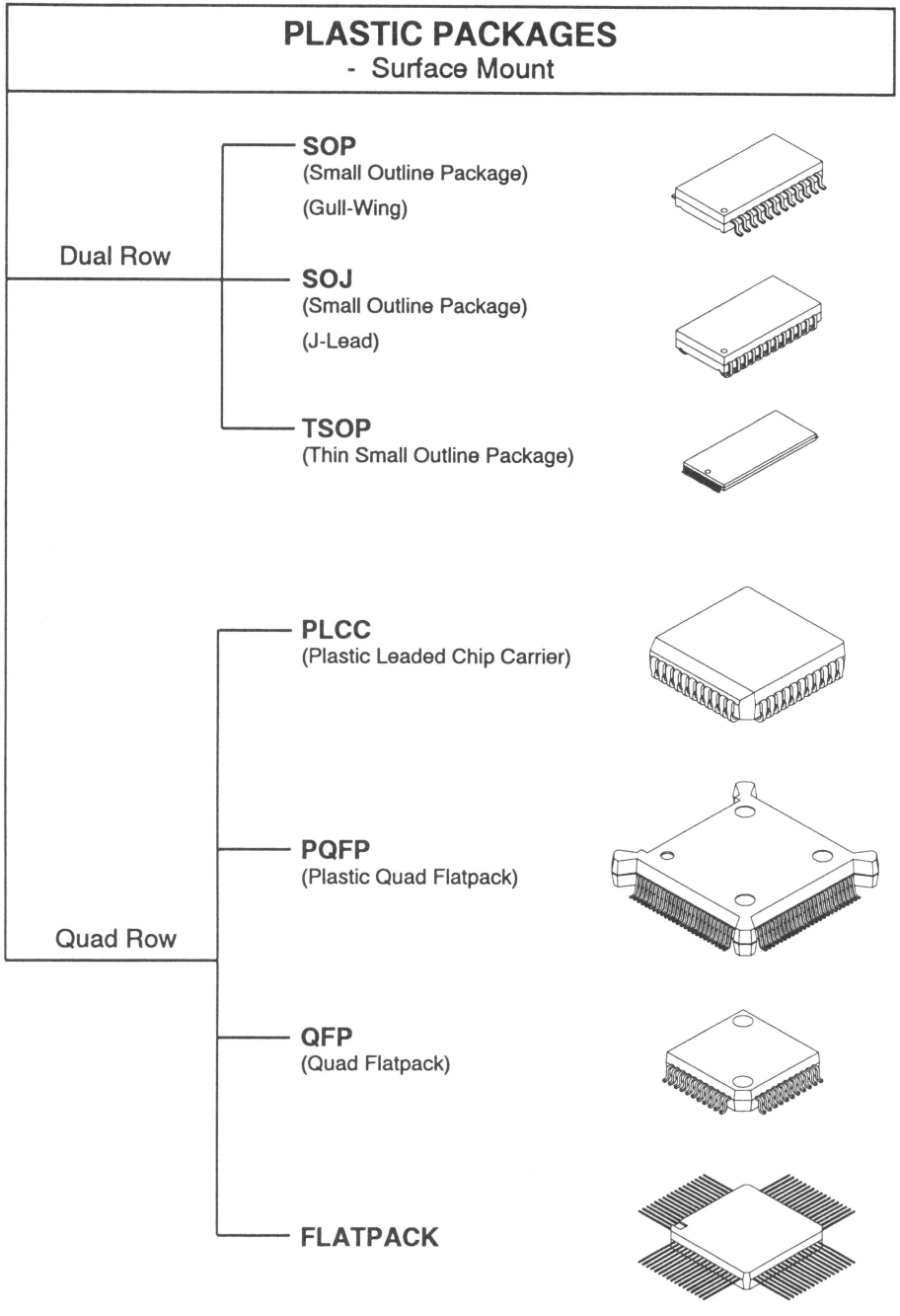
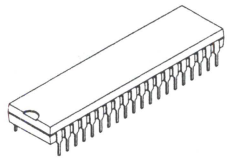


PACKAGE TYPES (Continued)

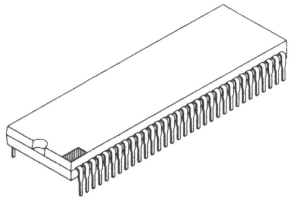
PLASTIC PACKAGES
- Insertion Mount

Dual Row

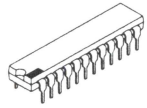
P-DIP
(Plastic Dual In-Line Package)



SHRINK DIP
(Shrink Dual In-Line Package)



SKINNY DIP
(Skinny Dual In-Line Package)



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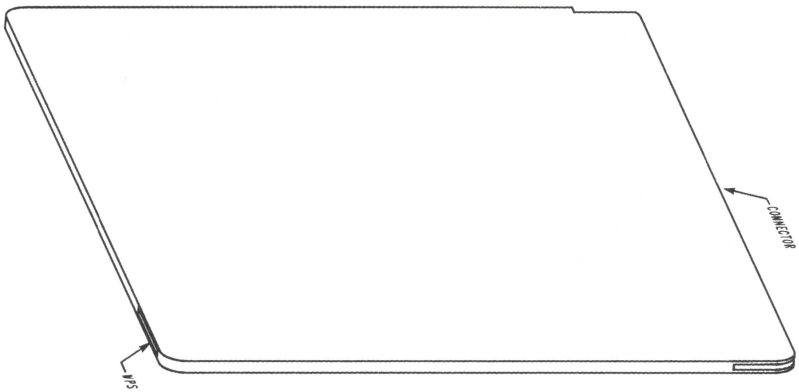
PACKAGE TYPES (Continued)

PCMCIA PC CARD—TYPE I AND TYPE II

Type I



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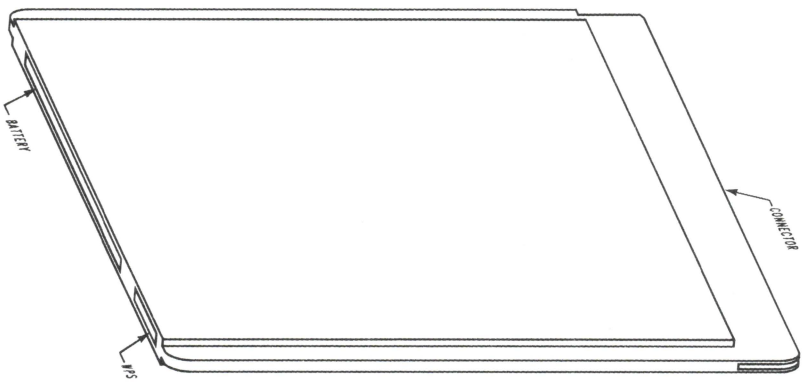
Type II



240817-6

CERAMIC PACKAGE ATTRIBUTES

Ceramic Dual In-Line Package (C-DIP)								
Lead Count	16	18	22	24	28	32	40	48
Sq./Rect.	R	R	R	R	R	R	R	R
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.109	0.109	0.109	*0.130 0.100	*0.132 0.102	0.120	*0.154 0.123	*0.172 0.142
Weight (gm)	1.41	1.62	1.89	2.22	4.56			8.43
Max. Footprint (inches)								
UV Eraseable				X	X	X	X	X
Shipping Media Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X
Desiccant Package								
Comments/ Footnotes	*EPROM Lid							

CERAMIC PACKAGE ATTRIBUTES (Continued)

Leadless Chip Carrier (LCC)							
Lead Count	18	20	28	32	44	68	68
Sq./Rect.	R	R	S	R	S	S	S
Pitch (inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.068	0.068	0.073	*0.080 0.108	*0.092 0.120	0.096	0.130
Weight (gm)		0.70	1.18	1.02	2.33	4.67	4.67
Max. Footprint (inches)							
UV Eraseable	X	X	X	See Note	See Note		X
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X
Desiccant Pack							
Comments/ Footnotes	32L— 0.080 = Solid Lid, Non-UV. 32L— 0.108 = EPROM Lid, UV. 44L— 0.092 = Solid Lid, Non-UV. 44L— 0.120 = EPROM Lid, UV.						

Pin Grid Array (PGA)											
Lead Count	68	68	68	88	88	88	132	168	208	240–280	272–320
Sq./Rect.	S	S	*S	S	S	*S	S	S	S	S	S
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.105	0.110	0.125	0.105	0.110	0.125	0.110	0.110	0.110	0.110	0.110
Weight (Gm)	8.69	8.69	8.69	10.43	10.43	10.43	16.07				
Max. Footprint (inches)	1.15	1.15	1.15	1.35	1.35	1.35	1.450	1.750	1.750	1.950	2.16
UV Eraseable			X			X					
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X	X	X
Desiccant Pack											
Comments/ Footnotes	*With EPROM										

CERAMIC PACKAGE ATTRIBUTES (Continued)

Ceramic Quad Flatpack (CQFP)			
Lead Count	68	164	196
Sq./Rect.	S	S	S
Pitch (inches)	0.050	0.025	0.025
Package Thickness (inches)			
Weight (gm)	12*	12*	17*
Max. Footprint (inches)			
UV Eraseable	X		
Shipping Media: Carrier Tape & Reel Trays	X	X	X X
Desiccant Pack			
Comments/ Footnotes	*Weighed with tie bar attached.		

CERDIP									
Lead Count	16	18	20	22	24	28	32	40	42
Sq./Rect.	R	R	R	R	R	R	R	R	R
Pitch (mm)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.157	0.157	0.153	0.165	0.165	0.167	0.167	0.167	0.167
Weight (gm)	2.1		2.87	4.39	6.69	8.68	9.81	12.03	
Max. Footprint (inches)									
UV Eraseable	X	X	X	X	X	X	X	X	X
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X
Desiccant Pack									
Comments/ Footnotes	Available with or without UV Window. Weights are without UV Window.								

CERAMIC PACKAGE ATTRIBUTES (Continued)

Ceramic QuadPack (CERQUAD)			
Lead Count	44	52	68
Sq./Rect.	S	S	S
Pitch (inches)	0.050	0.050	0.050
Package Thickness (inches)	0.172	0.172	0.172
Weight (gm)	2.85	3.59	7.14
Max. Footprint (inches)	0.72	0.82	1.02
UV Eraseable	X	X	X
Shipping Media: Tubes Tape & Reel Trays	X	X	X
Desiccant Pack			
Comments/ Footnotes	Available with or without UV Window		

PLASTIC PACKAGE ATTRIBUTES

Plastic Dual In-Line (PDIP)									
Lead Count	16	18	20	24	28	32	40	48	64
Sq./Rect.	R	R	R	R	R	R	R	R	R
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.132	0.132	0.132	0.152	0.152	0.150	0.160	0.162	0.167
Weight (gm)	1.045	1.248	1.418	1.67	1.94	4.815	6.128	7.912	12.05
Max. Footprint (inches)									
UV Eraseable									
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X
Desiccant Pack									
Comments/ Footnotes	Some pin counts available in; Halflead, Widebody; Widebody; and Standard Type P.								

PLASTIC PACKAGE ATTRIBUTES (Continued)

Plastic (Flatpack)	
Lead Count	68
Sq./Rect.	S
Pitch (inches)	0.050
Package Thickness (inches)	0.168
Weight (gm)	5.6
Max. Footprint (inches)	
UV Eraseable	
Shipping Media: Tubes Tape & Reel Carrier	 X
Desiccant Pack	
Comments/ Footnotes	Through Hole Use Only

Plastic Quad Flatpack (PQFP)					
Lead Count	84	100	132	164	196
Sq./Rect.	S	S	S	S	S
Pitch (inches)	0.025	0.025	0.025	0.025	0.025
Package Thickness (inches)	0.170	0.170	0.170	0.170	0.170
Weight (gm)	2.07	2.8	4.2	6.1	8.55
Max. Footprint (inches)					
UV Eraseable					
Shipping Media: Tubes Tape & Reel Trays	 X X X	 X X X	 X X X	 X X X	 X X X
Desiccant Pack	X	X	X	X	X
Comments/ Footnotes	All PQFPs are "Gull Wing" with bumpers *MM-PQFP				

PLASTIC PACKAGE ATTRIBUTES (Continued)

Quad Flatpack												
Lead Count	44	48	64	80	80	100	100	128	144	160	176	208
Sq./Rect.	S	S	S	S	R	S	R	S	S	S	S	S
Pitch (mm)	0.800	0.800	0.650	0.500	0.800	0.50	0.80	0.80	0.5	0.65	0.5	0.500
Package Thickness (mm)	2.35	2.55	2.55	1.66	3.15	1.66	3.15	3.65	1.5	3.65	1.5	3.56
Weight (gm)	0.42		0.71	0.50	1.65	0.64	1.65					5.18
Max. Footprint (inches)												
UV Eraseable												
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X	X	X	X
Desiccant Pack	X	X	X	X	X	X	X	X	X	X	X	X
Comments/ Footnotes	Gull Wing Lead Configuration, non-bumpered											

Plastic Leaded Chip Carrier (PLCC)								
Lead Count	20	28	28	32	44	52	68	84
Sq./Rect.	S	S	R	R	S	S	S	S
Pitch (inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.152	0.152	0.108	0.108	0.148	0.150	0.150	0.150
Weight (gm)	0.705	1.15	0.85	1.1	2.31	3.17	4.8	6.2
Max. Footprint (inches)	0.390	0.490	See Note	See Note	0.690	0.790	0.990	0.190
UV Eraseable								
Shipping Media: Tubes Tape & Reel Trays	X X X	X X X	X X X	X X X	X X X	X	X X X	X X X
Desiccant Pack	X	X	X	X	X	X	X	X
Comments/ Footnotes	All PLCC's are "J" Lead 28R— 0.39 x 0.59 32R— 0.49 x 0.59							

PLASTIC PACKAGE ATTRIBUTES (Continued)

Small Outline Package (SOJ)		
Lead Count	20	24
Sq./Rect.	R	R
Pitch (mm)	1.27	1.27
Package Thickness (Inches)	0.105	0.113
Weight (gm)	0.50	0.62
Max. Footprint Inches	0.300	0.300
UV Eraseable		
Shipping Media: Tubes Tape & Reel Trays	 X X	 X X
Desiccant Pack	X	X
Comments/ Footnotes	"J" Lead Configuration	

Small Outline Package (SOP)			
Lead Count	28	32	44
Sq./Rect.	R	R	R
Pitch (mm)	1.27	1.27	1.27
Package Thickness (mm)	2.74	2.18	2.30
Weight (gm)	0.70		
Max. Footprint (inches)	0.330		
UV Eraseable			
Shipping Media: Tubes Tape & Reel Trays	X	X	X
Desiccant Pack	X	X	X
Comments/ Footnotes	Gull Wing Lead Configuration		

PLASTIC PACKAGE ATTRIBUTES (Continued)

Thin Small Outline Package (TSOP)			
Lead Count	32	40	56
Sq./Rect.	R	R	R
Pitch (mm)	0.50	0.50	0.50
Package Thickness (mm)	1.2	1.0	1.0
Weight (gm)	0.37		
Max. Footprint (mm)			
UV Eraseable			
Shipping Media: Tubes Tape & Reel Trays	X	X	X
Desiccant Pack		TBD	TBD
Comments/ Footnotes	TSOP is "Gull Wing" Configuration		

MODULE ATTRIBUTES

Single In-Line Leaded Memory Module (SIP)	
Lead Count	30
Sq./Rect.	R
Pitch (mm)	2.54
Package Thickness (inches)	2.00
Weight (gm)	
Max. Footprint (inches)	3.10
UV Eraseable	
Shipping Media: Tubes Tape & Reel Trays	 X
Desiccant Pack	
Comments/ Footnotes	Insertable Module

Single In-Line Leadless Memory Module (SIMM)		
Lead Count	30	80
Sq./Rect.	R	R
Pitch (inches)	0.100	0.050
Package Thickness (inches)	0.20	0.33
Weight (gm)		15.7
Max. Footprint (inches)	3.50	4.65
UV Eraseable		
Shipping Media: Tubes Tape & Reel Trays	 X	 X
Desiccant Pack		
Comments/ Footnotes	JEDEC Standard Insertable Module	

PACKAGE/MODULE/PC CARD SELECTION GUIDE

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
Ceramic Dual-In-Line (C-DIP), 0.100″ Pitch, Socket or Insertion Mount 24, 28, 40, 48 C-DIP's Available with EPROM or Solid Lid 32 C-DIP Available with EPROM (Lid) Only	16	C	
	18	C	
	22	C	
	24	C	
	28	C	
	32	C	
	40	C	
	48	C	
Ceramic Leadless Chip Carrier (LCC), 0.050″ Pitch, Socket or Surface Mount 32, 44, and 68 LCC's Available with EPROM or Solid Lid	18	R	
	20	R	
	28	R	
	32	R	
	44	R	
	68	R	
Ceramic Pin Grid Array (PGA), 0.100″ Pitch, Socket or Insertion Mount 68L and 88L "Cavity Up" Available with EPROM or Solid Lid	68	A	
	88	A	
	88	A	Cavity Down
	132	A	Cavity Down
	168	A	Cavity Down
	208	A	Cavity Down
	240–280	A	Cavity Down
	272–320	A	Cavity Down
Ceramic Quad Flatpack (CQFP), 68L Available in 0.050″ Pitch. 164L and 196L Available in 0.025″ Pitch, Socket or Surface Mount	68	Q	Flat Leads
	164	K	Flat Leads
	196	K	Flat Leads
Ceramic DIP (CERDIP), 0.100″ Pitch, Socket or Insertion Mount	16	D	
	18	D	
	20	D	
	22	D	
	24	DP	300 Mil
	24	D	
	28	DP	300 Mil
	28	D	
	32	D	
	40	D	
	42	D	

PACKAGE/MODULE/PC CARD SELECTION GUIDE (Continued)

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
CERQUAD, 0.050″ Pitch, Socket Mount, All Leadcounts Offer UV Window	44	J	
	52	J	
	68	J	
Plastic Dual-In-Line (PDIP), 0.100″ Pitch, 64L "Shrink DIP" has a 0.070″ Pitch Socket and Insertion Mount	16	P	
	18	P	
	20	P	
	24	P	
	24	PD	300 Mil
	28	P	
	28	PD	300 Mil
	32	P	
	40	P	
	48	P	
	64	U	Shrink
Plastic Flatpack (PFP), 0.050″ Pitch Shipped in Carrier with Flat Leads, Through-Hole Mount	68	FP	
Plastic Leaded Chip Carrier (PLCC), 0.050″ Pitch Surface or Surface Mount 28L is Available in a Square and Rectangular Package Body 32L is Available in a Rectangular Package Body Only	20	N	Sq.
	28	N	Sq./Rect.
	32	N	Rect.
	44	N	Sq.
	52	N	Sq.
	68	N	Sq.
	84	N	Sq.
Plastic Quad Flatpack (PQFP), 0.025″ Pitch, Surface Mount Some Packages Available in a Variety of Options: Die Up, Die Down, and Die Down with Heatspreader	84	KD	
	100	KD, KU, NG	
	132	KD, KU, NG	
	164	KU	
	196	KU	
Quad Flatpack (QFP), Variable Lead Pitch Surface Mount.	44	S	
	48	S	
	64	S	
	80	SB, S	Sq./Rect.
	100	SB, S	Sq./Rect.
	128	S	
	144	SB	
	160	S	
	176	SB	
	208	SB	
Quad Flatpack (QFP), Surface Mount, Copper Lead Frame	208	SB	

PACKAGE/MODULE/CARD SELECTION GUIDE (Continued)

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
Small Outline J-Lead (SOJ), 1.27mm Pitch Surface Mount	20 24	PE PE	
Small Outline Package (SOP), 1.27mm Pitch Surface Mount	28 32 44	PA PA PA	
Thin Small Outline Package (TSOP), 0.50mm Pitch, Surface Mount Available in Die Up or Die Down	32 40 56	E, F E, F E, F	
Single In-Line Leaded Memory Module (SIP), 2.54mm Pitch, Socket or Insertion Mount	30	GB	
Single In-Line Leadless Memory Module (SIMM) 0.100″ Pitch, Socket Mount	30 80	SM SM	

ExCA	PCMCIA/JEIDA 68-Pin Int'l Std	Devices
PCMIA 2.0 Card (Type I)	68	iMC00XFLKA
PCMCIA 2.0 Card (Type II)	68	iNC110XX

REVISION SUMMARY

The main differences between 240817-004 revision and the -003 version are following:

- Deleted LGA
- Deleted ZIP

Package/Module/PC Card Outlines and Dimensions

2

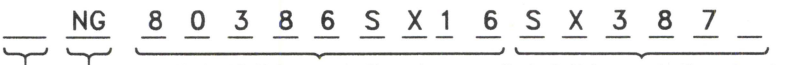
Package/Module/PC Card Outlines and Dimensions

2

October 1993

Order Number: 231369-010

Intel Product Identification Codes



Package Type

A	–	Ceramic Pin Grid Array
B	–	Ceramic Land Grid Array
C	–	Ceramic Dual In-Line Package
D	–	Cerdip Dual In-Line Package
DP	–	Cerdip Dual In-Line Package, 300 MIL
E	–	Thin Small Out-Line Package, Die Up
F	–	Thin Small Out-Line Package, Die Down
FP	–	Plastic Flatpack Package
GB	–	Single In-Line Leaded Memory Module
J	–	Cerquad Package
K	–	Ceramic Quad Flatpack Package, Fine Pitch, Flat Leads
KD	–	Plastic Quad Flatpack Package, Fine Pitch, Die Down
KU	–	Plastic Quad Flatpack Package, Fine Pitch, Die Up
N	–	Plastic Leaded Chip Carrier
NG	–	Plastic Quad Flatpack, Fine Pitch, Die Down w/ Heat spreader
P	–	Plastic Dual In-Line Package
PA	–	Small Out-Line "Gull-Wing" Package
PD	–	Plastic Dual In-Line Package, 300 MIL
PE	–	Small Out-Line "J"-Lead Package
Q	–	Ceramic Quad Flatpack Package
R	–	Ceramic Leadless Chip Carrier
S	–	Quad Flatpack Package
SB	–	Shrink Quad Flatpack Package
SM	–	Single In-Line Leadless Memory Module
U	–	Plastic Dual In-Line Package, Shrink Dip
X	–	Unpackaged Devices
Z	–	Zigzag In-Line Package

A	–	Indicates automotive operating temperature range
I	–	Indicates industrial grade
L	–	Indicates extended operating temperature range (−40°C to +85°C) express product with 160 ± 8 hrs. dynamic burn-in.
Q	–	Indicates commercial temperature range (0°C to 70°C) express product with 160 ± 8 hrs. dynamic burn-in.
T	–	Indicates extended temperature range (−40°C to +85°C) express product without burn-in.

231369-1

EXAMPLES:

A80486DX25SX387 32-Bit Microprocessor, 25 MHz, 168-Lead Ceramic Pin Grid Array
NG80386SX16SX159 16-Bit Microprocessor, 16 MHz, 100-Lead Plastic Quad Flatpack

Package/Module/PC Card Outlines and Dimensions

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CERAMIC SIDEBRAZE DUAL IN-LINE PACKAGE

Symbol List for Ceramic Side Braze Dual In-Line Family

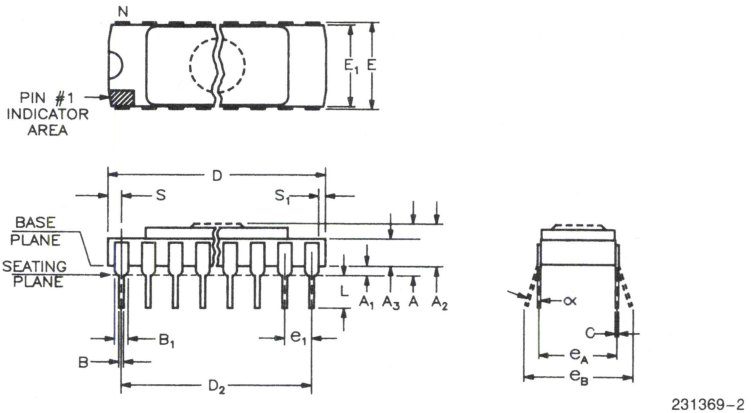
Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_2	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E_1	Body width dimensions not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B_1" is nominal.

Packaging Family Attributes	
Category	Ceramic Dual-In-Line
Acronym	C-DIP or Side Brazed
Lead Configuration	Sidebraze
Lead Counts	16, 18, 22, 24, 32, 40, 48
Lead Finish	Gold Plate
Lead Pitch	0.100″
Board Assembly Type	Socket and Insertion Mount

NOTES:
1. Alloy 42 or Kovar Leads.
2. Multilayer Co-Fired Ceramic Body.

16 LEAD CERAMIC DUAL IN-LINE PACKAGE



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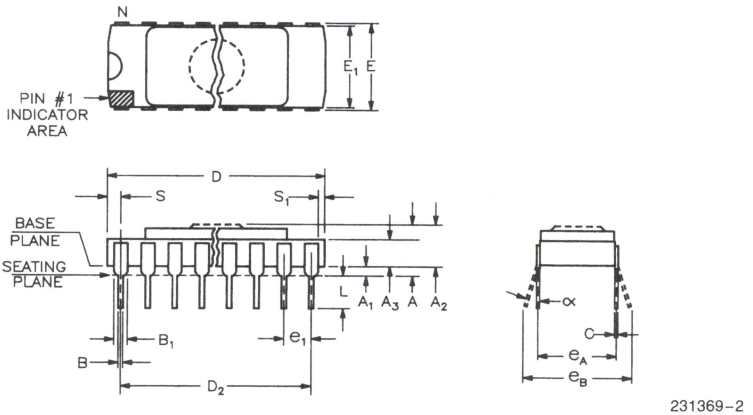
Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A_1	0.64	1.27		0.025	0.050	
A_2	2.16	3.40		0.085	0.134	
A_3	1.91	3.05		0.075	0.120	
B	0.38	0.56		0.015	0.022	
B_1	1.37		Typical	0.054		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	20.07	20.57		0.790	0.810	
D_2	17.78		Reference	0.700		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.37	7.62		0.290	0.300	
e_1	2.29	2.79		0.090	0.110	Typical
e_A	7.37		Reference	0.290		Reference
e_B	7.62	8.38		0.300	0.330	
L	3.18	4.06		0.125	0.160	
N	16			16		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

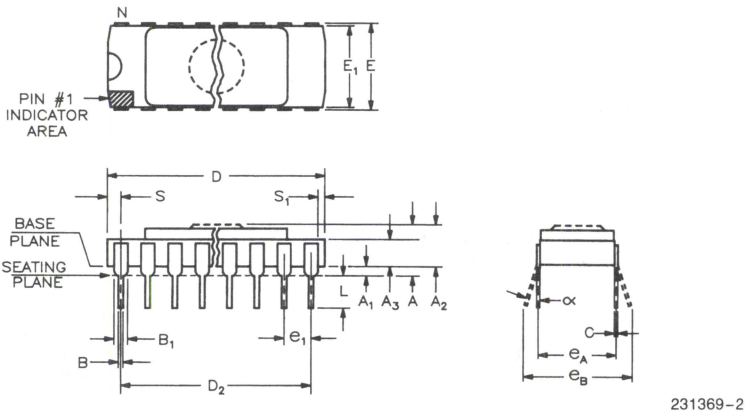
18 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A_1	0.64	1.27		0.025	0.050	
A_2	2.16	3.40		0.085	0.134	
A_3	1.91	3.05		0.075	0.120	
B	0.38	0.56		0.015	0.022	
B_1	1.37		Typical	0.054		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.61	23.11		0.890	0.910	
D_2	20.32		Reference	0.800		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.37	7.62		0.290	0.300	
e_1	2.29	2.79		0.090	0.110	
e_A	7.37		Reference	0.290		Reference
e_B	7.62	8.38		0.300	0.330	
L	3.18	4.06		0.125	0.160	
N	18			18		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

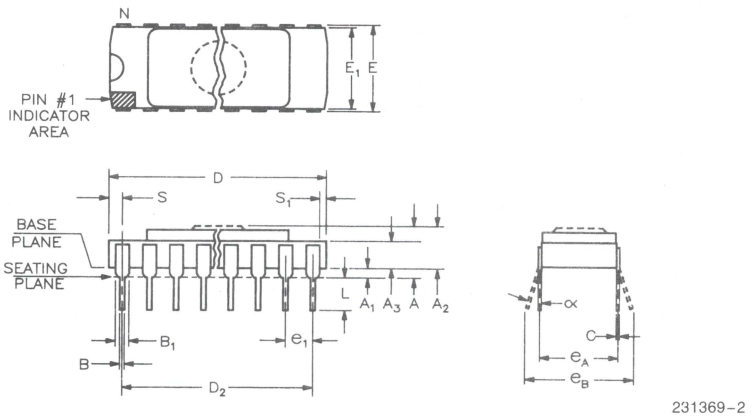
22 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A_1	0.64	1.27		0.025	0.050	
A_2	2.16	3.40		0.085	0.134	
A_3	2.03	3.05		0.080	0.120	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	27.56	28.32		1.085	1.115	
D_2	25.40		Reference	1.000		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.37	7.62		0.290	0.300	
e_1	2.29	2.79		0.090	0.110	
e_A	7.37		Reference	0.290		Reference
e_B	7.62	9.14		0.300	0.360	
L	3.18	4.06		0.125	0.160	
N	22			22		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

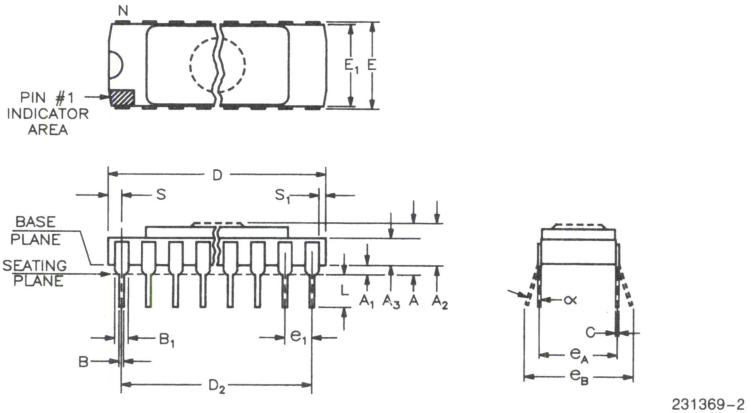
24 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.18	4.44	Solid Lid	0.125	0.175	Solid Lid
A	3.81	5.33	EPROM Lid	0.150	0.210	EPROM Lid
A_1	1.02	1.52		0.040	0.060	
A_2	2.16	2.92	Solid Lid	0.085	0.115	Solid Lid
A_2	2.79	3.81	EPROM Lid	0.110	0.150	EPROM Lid
A_3	1.91	2.54		0.075	0.100	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	30.10	30.86		1.185	1.215	
D_2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.86	15.37		0.585	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.15		0.600	0.665	
L	3.18	4.06		0.125	0.160	
N	24			24		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

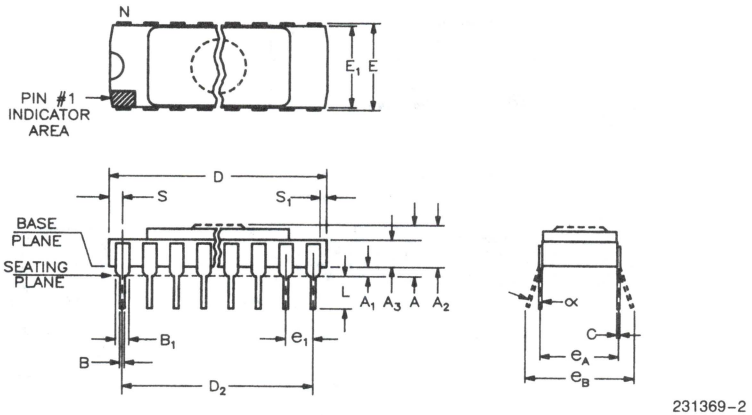
28 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.30	4.44	Solid Lid	0.130	0.175	Solid Lid
A	3.94	5.33	EPROM Lid	0.155	0.210	EPROM Lid
A_1	1.02	1.52		0.040	0.060	
A_2	2.29	2.92	Solid Lid	0.090	0.115	Solid Lid
A_2	2.92	3.81	EPROM Lid	0.115	0.150	EPROM Lid
A_3	2.03	2.54		0.080	0.100	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	35.18	35.94		1.385	1.415	
D_2	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.86	15.37		0.585	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	28			28		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

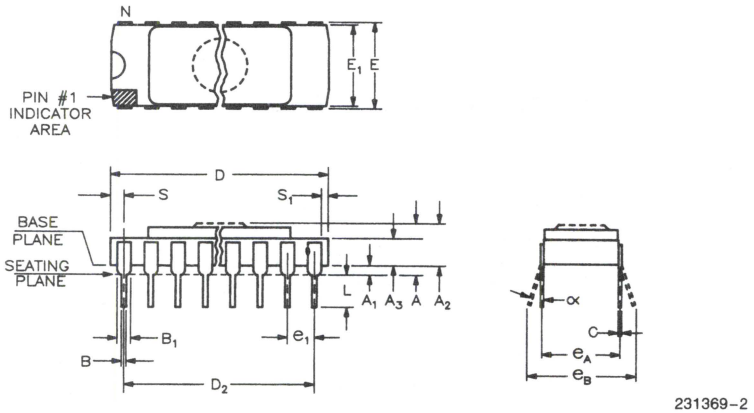
32 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.94	5.23	EPROM Lid	0.155	0.206	EPROM Lid
A_1	1.02	1.52		0.040	0.060	
A_2	3.00	3.71	EPROM Lid	0.118	0.146	EPROM Lid
A_3	2.03	2.54		0.080	0.100	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	40.28	41.00		1.586	1.614	
D_2	38.10		Reference	1.500		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.86	15.37		0.585	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	32			32		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

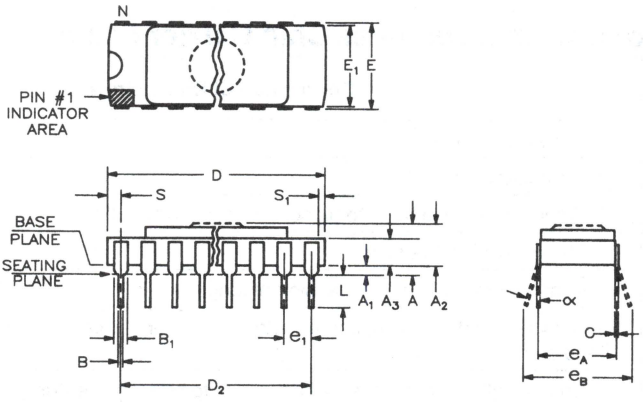
40 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.30	5.51	Solid Lid	0.130	0.217	Solid Lid
A	4.04	6.58	EPROM Lid	0.159	0.259	EPROM Lid
A_1	1.02	1.52		0.040	0.060	
A_2	2.29	3.99	Solid Lid	0.090	0.157	Solid Lid
A_2	3.02	4.87	EPROM Lid	0.119	0.190	EPROM Lid
A_3	2.03	3.66		0.080	0.144	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	50.29	51.31		1.980	2.020	
D_2	48.26		Reference	1.900		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.86	15.37		0.585	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	40			40		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

48 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.24	5.51	Solid Lid	0.167	0.217	Solid Lid
A	4.95	6.32	EPROM Lid	0.195	0.249	EPROM Lid
A_1	1.02	1.52		0.040	0.060	
A_2	3.23	3.99	Solid Lid	0.127	0.157	Solid Lid
A_2	3.94	4.80	EPROM Lid	0.155	0.189	EPROM Lid
A_3	2.95	3.66		0.116	0.144	
B	0.38	0.56		0.015	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	60.45	61.47		2.380	2.420	
D_2	58.42		Reference	2.3		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.86	15.37		0.585	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	16.89		0.600	0.665	
L	3.18	4.06		0.125	0.160	
N	48			48		
S	0.76	1.78		0.030	0.070	
S_1	0.13			0.005		

CERAMIC LEADLESS CHIP CARRIER

Symbol List for Ceramic Leadless Chip Carrier Family

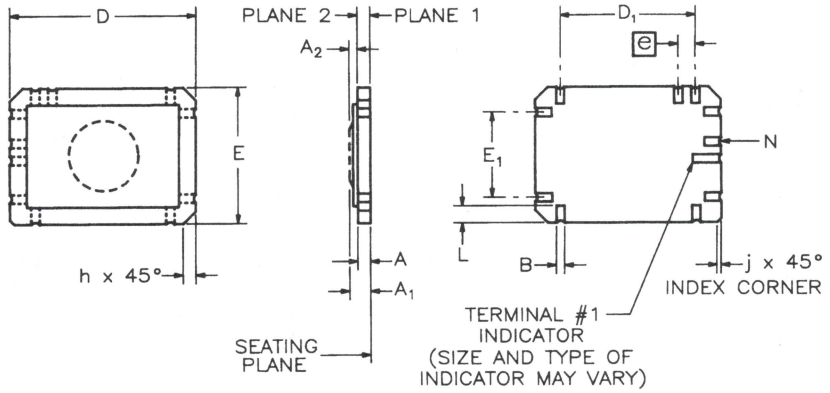
Letter or Symbol	Description of Dimensions
A	Thickness of base body
A_1	Total package height
A_2	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package dimension of length
D_1, E_1	A body length dimension, corner cutout to corner cutout or end lead center to end lead center
D_2, E_2	A body length dimension, end lead center to end lead center
D_3, E_3	A body length dimension, corner cutout to index corner cutout
D_4, E_4	Ceramic body fixture
E	Largest overall package dimension of width
e	Linear spacing
e_1	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	The total number of potentially useable lead positions
R_1	Inner notch radius

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.
5. Corner configuration optional.

Packaging Family Attributes	
Category	Ceramic Leadless Chip Carrier
Acronym	LCC
Lead Configuration	N/A
Lead Counts	18, 20, 28, 32, 44, 68
Lead Finish	Gold Plate
Lead Pitch	0.050"
Board Assembly Type	Socket and Surface Mount

NOTES:
1. 68L not certified for Surface Mount, must be socketed.
2. Multilayer Co-Fired Ceramic Body.

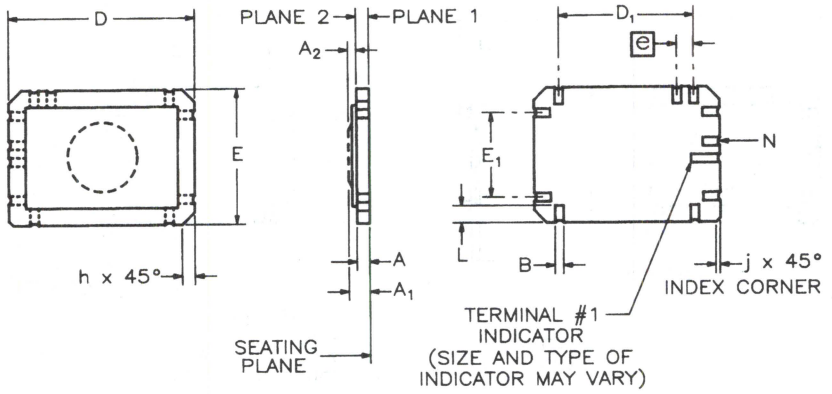
18 CERAMIC LEADLESS CHIP CARRIER



231369-8

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A_1	1.60	1.88		0.063	0.074	
A_2	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	10.54	11.18		0.415	0.440	
D_1	5.08		Reference	0.200		Reference
E	6.99	7.62		0.275	0.300	
E_1	3.81		Reference	0.150		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	18			18		

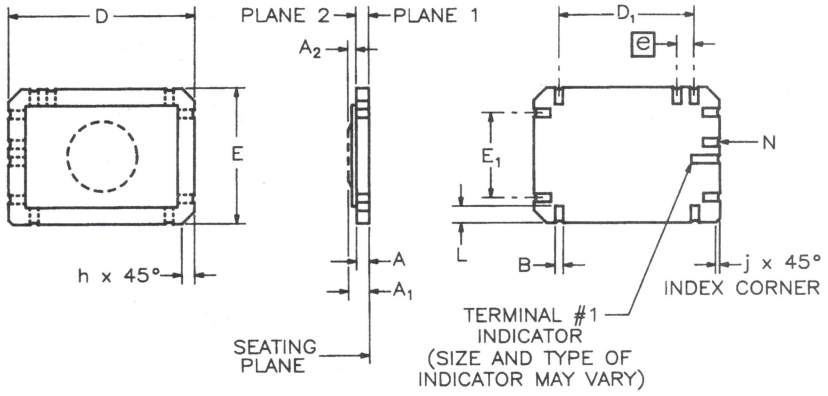
20 CERAMIC LEADLESS CHIP CARRIER



231369-8

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A_1	1.60	1.88		0.063	0.074	
A_2	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	10.54	11.18		0.415	0.440	
D_1	6.35		Reference	0.250		Reference
E	7.11	7.62		0.280	0.300	
E_1	3.81		Reference	0.150		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	20			20		

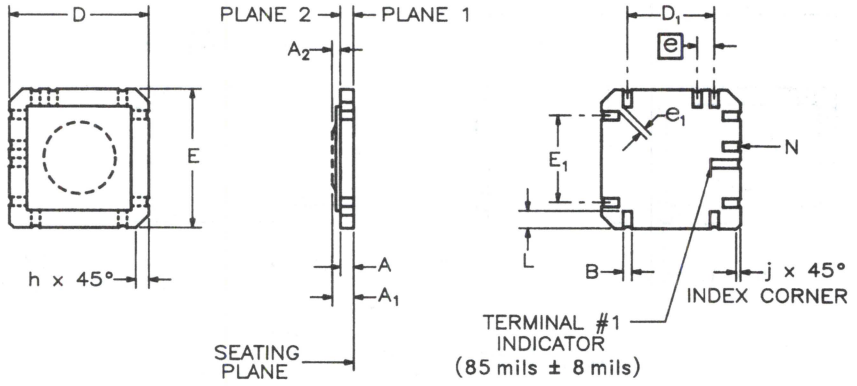
32 CERAMIC LEADLESS CHIP CARRIER



231369-8

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.45	2.03		0.057	0.080	
A_1	1.70	2.39	Solid Lid	0.067	0.094	Solid Lid
A_1	2.39	3.12	EPROM Lid	0.094	0.123	EPROM Lid
A_2	0.25	0.36	Solid Lid	0.010	0.014	Solid Lid
A_2	0.94	1.09	EPROM Lid	0.037	0.043	EPROM Lid
B	0.51	0.76		0.020	0.030	
D	13.72	14.22		0.540	0.560	
D_1	10.16		Reference	0.400		Reference
E	11.18	11.68		0.440	0.460	
E_1	7.62		Reference	0.300		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	32			32		

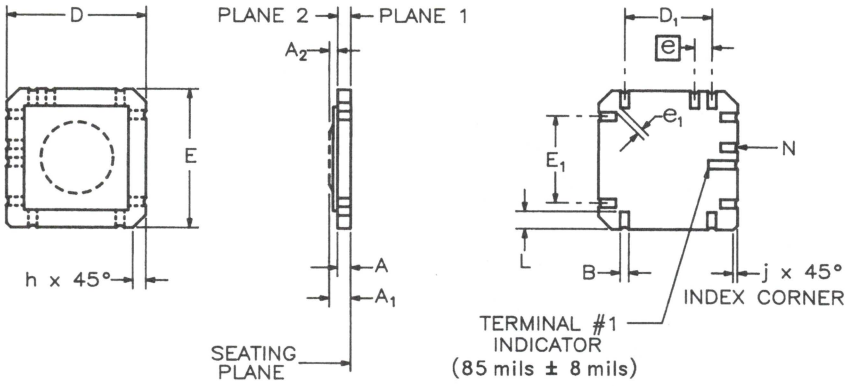
28 CERAMIC LEADLESS CHIP CARRIER



231369-9

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A_1	1.60	2.13		0.063	0.084	
A_2	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	11.18	11.68		0.440	0.460	
D_1	7.62		Reference	0.300		Reference
E	11.18	11.68		0.440	0.460	
E_1	7.62		Reference	0.300		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.045	0.055	
N	28			28		

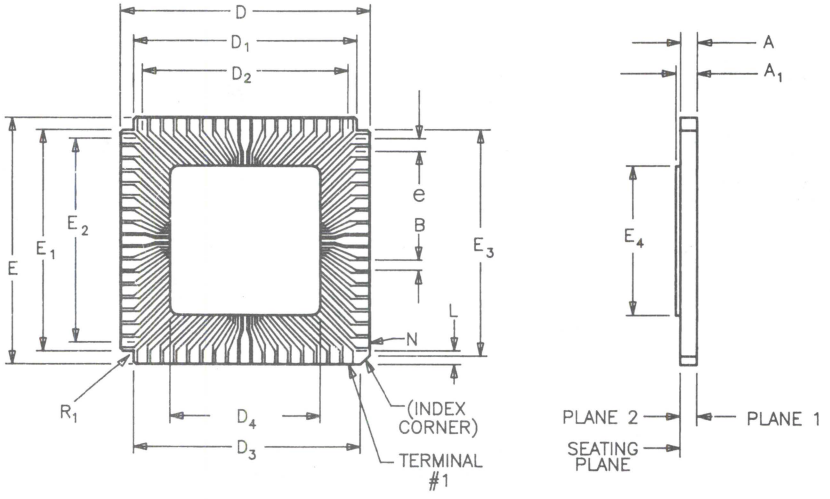
44 CERAMIC LEADLESS CHIP CARRIER



231369-9

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.52	2.54		0.060	0.100	
A_1	1.78	2.90	Solid Lid	0.070	0.114	Solid Lid
A_1	2.46	3.63	EPROM Lid	0.097	0.143	EPROM Lid
A_2	0.25	0.36	Solid Lid	0.010	0.014	Solid Lid
A_2	0.94	1.09	EPROM Lid	0.037	0.043	EPROM Lid
B	0.51	0.76		0.020	0.030	
D	16.13	16.89		0.635	0.665	
D_1	12.70		Reference	0.500		Reference
E	16.13	16.89		0.635	0.665	
E_1	12.70		Reference	0.500		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	44			44		

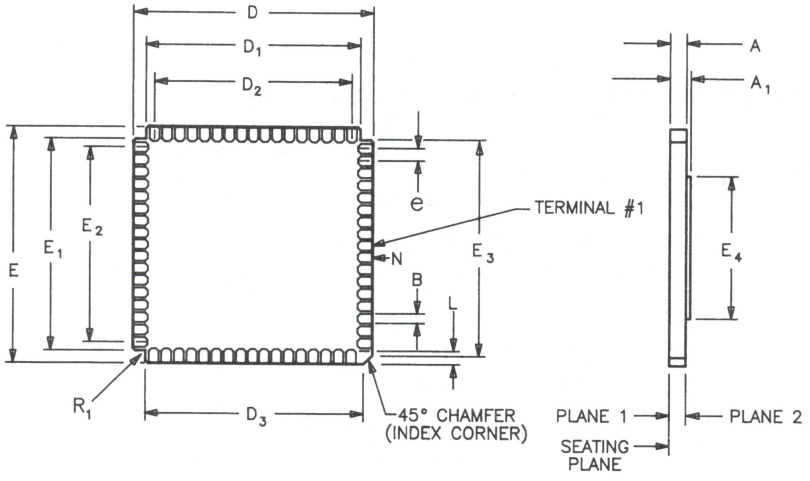
68 CERAMIC LEADLESS CHIP CARRIER VARIATION: DIE DOWN



231369-10

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.37	1.68		0.054	0.066	
A_1	2.16	2.72		0.085	0.107	
B	0.84	0.99	Typical	0.033	0.039	Typical
D	23.88	24.38		0.940	0.960	
D_1	21.39	21.39		0.842	0.858	
D_2	20.32		Reference	0.800		Reference
D_3	21.92		Reference	0.863		Reference
D_4	16.76	17.27		0.660	0.680	
E	23.88	24.38		0.940	0.960	
E_1	21.39	21.79		0.842	0.858	
E_2	20.32		Reference	0.800		Reference
E_3	21.92		Reference	0.863		Reference
E_4	16.76	17.27		0.660	0.680	
e	1.04	1.50	Typical	0.041	0.059	Typical
L	0.94			0.037		
N	68			68		
R_1		0.25			0.010	

68 CERAMIC LEADLESS CHIP CARRIER VARIATION: DIE UP



231369-11

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.91	2.41		0.075	0.095	
A_1	2.92	3.68	W/EPROM	0.115	0.145	W/EPROM
B	0.84	1.12		0.033	0.044	
D	23.88	24.38		0.940	0.960	
D_1	21.39	21.79		0.842	0.858	
D_2	20.32		Reference	0.800		Reference
D_3	22.05		Reference	0.868		Reference
E	23.88	24.38		0.940	0.960	
E_1	21.39	21.79		0.842	0.858	
E_2	20.32		Reference	0.800		Reference
E_3	22.05		Reference	0.868		Reference
E_4	14.33	15.14		0.564	0.596	
e	1.04	1.50	Typical	0.041	0.059	Typical
L	1.27			0.050		
N	68			68		
R_1		0.25			0.010	

CERAMIC PIN GRID ARRAY PACKAGE

Symbol List for Ceramic Pin Grid Array Family

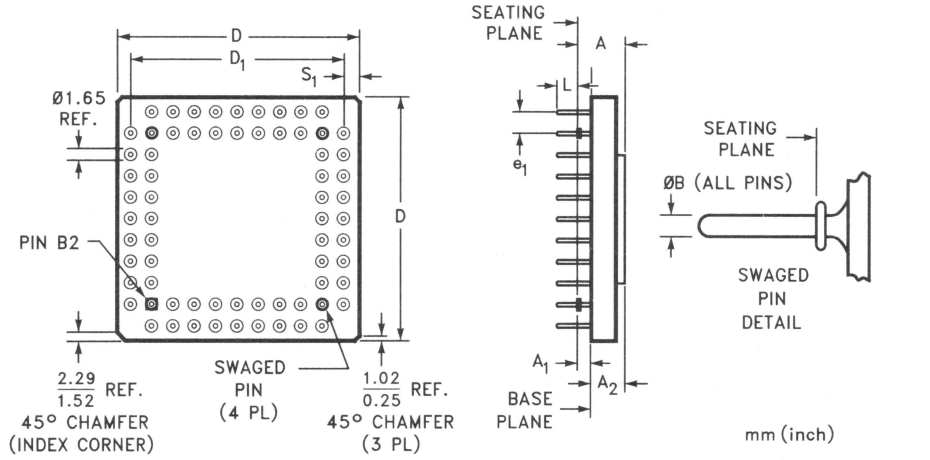
Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
A_4	Heat spreader thickness
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
D_2	Heat spreader length and width
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.
5. Details of Pin 1 identifier are optional.

Packaging Family Attributes	
Category	Ceramic Pin Grid Array
Acronym	C-PGA or PGA
Lead Configuration	Array
Lead Counts	68, 88, 132, 168–208, 240–280, 272–320
Lead Finish	Gold Plate, 60 Microinches of Gold over 100–350 Microinches of Nickel Plate
Lead Material	Kovar or Alloy 42
Lead Braze Material	Copper/Silver Eutectic
Lead Pitch	0.100″
Board Assembly Type	Socket and Insertion Mount

NOTES:
1. Alloy 42 or Kovar Leads.
2. Multilayer Co-Fired Ceramic Body.
3. 240–280 has variable pin count.

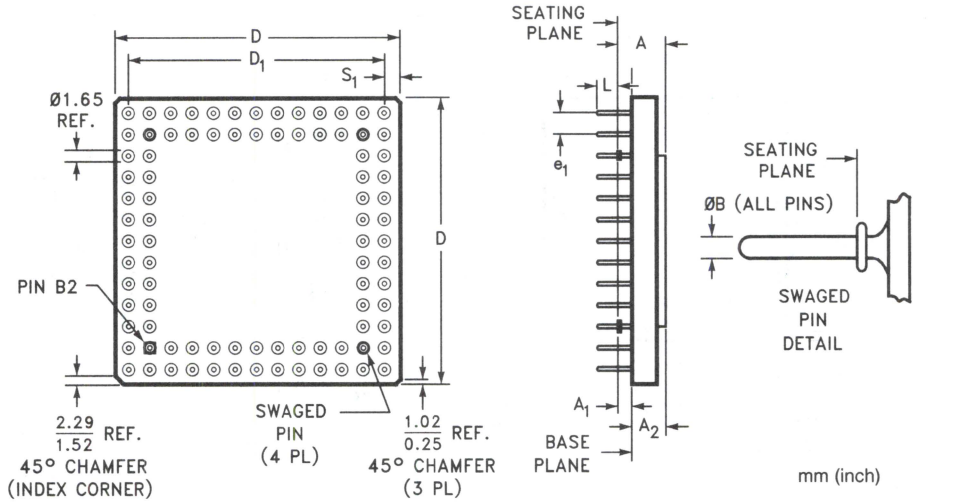
68 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-12

Family: Ceramic Pin Grid Array Package (Cavity Up)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.06	5.21	EPROM Lid	0.160	0.205	EPROM Lid
A	3.30	4.32	Solid Lid	0.130	0.170	Solid Lid
A_1	1.14	1.40		0.045	0.055	
A_2	2.16	3.18	Solid Lid	0.085	0.125	Solid Lid
A_2	2.67	3.94	EPROM Lid	0.105	0.155	EPROM Lid
B	0.43	0.51		0.017	0.020	
D	28.96	29.97		1.140	1.180	
D_1	25.27	25.53		0.995	1.005	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	68			68		
S_1	1.27	2.54		0.050	0.100	

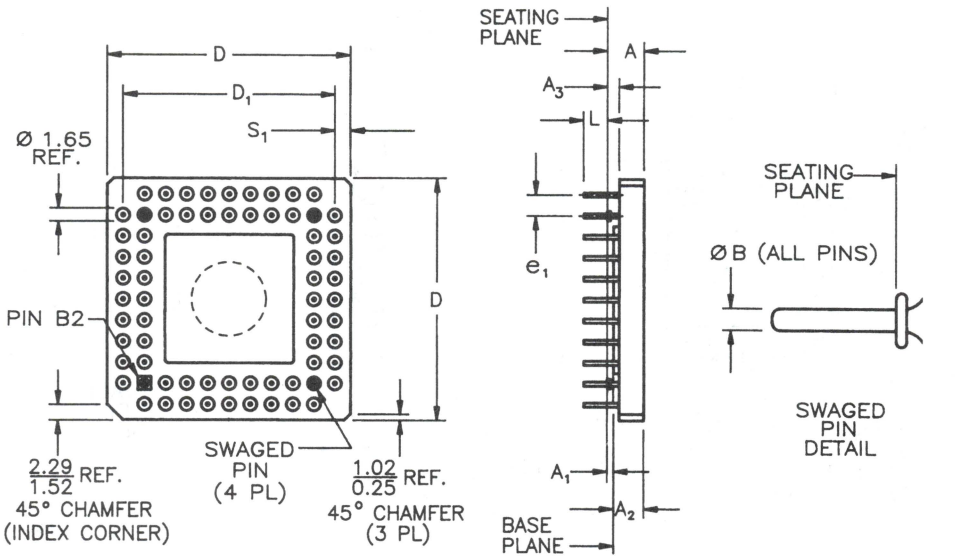
88 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-13

Family: Ceramic Pin Grid Array Package (Cavity Up)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.06	5.21	EPROM Lid	0.160	0.205	EPROM Lid
A	3.30	4.32	Solid Lid	0.130	0.170	Solid Lid
A_1	1.14	1.4		0.045	0.055	
A_2	2.16	3.18	Solid Lid	0.085	0.125	Solid Lid
A_2	2.67	3.94	EPROM Lid	0.105	0.155	EPROM Lid
B	0.43	0.51		0.017	0.020	
D	34.04	35.05		1.340	1.380	
D_1	30.35	30.61		1.195	1.205	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.56		0.120	0.140	
N	88			88		
S_1	1.27	2.54		0.050	0.100	

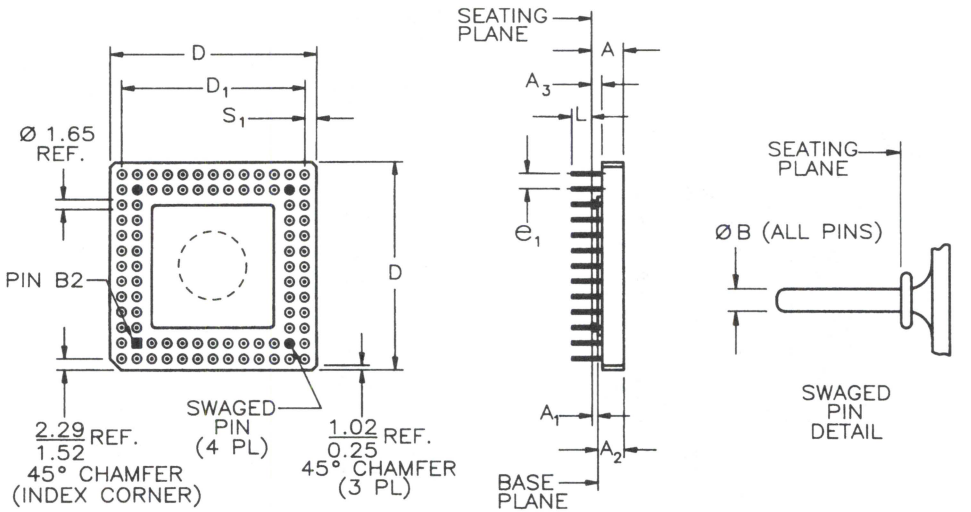
68 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-14

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_1		0.41	EPROM Lid		0.016	EPROM Lid
A_2	2.72	3.43	Solid Lid	0.107	0.135	Solid Lid
A_2	3.43	4.32	EPROM Lid	0.135	0.170	EPROM Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	28.95	29.97		1.140	1.180	
D_1	25.27	25.53		0.995	1.005	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	68			68		
S_1	1.27	2.54		0.050	0.100	

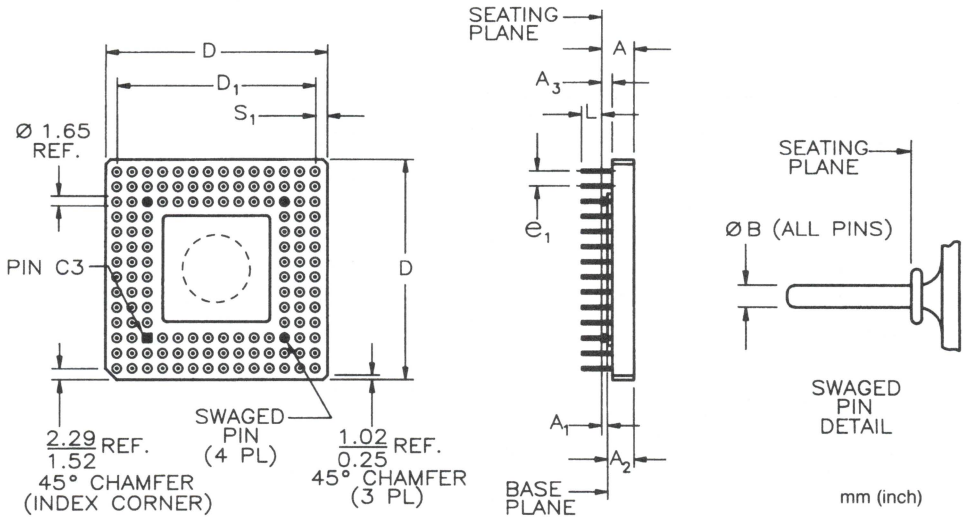
88 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-15

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	34.03	35.05		1.340	1.380	
D_1	30.35	30.61		1.195	1.205	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	88			88		
S_1	1.27	2.54		0.050	0.100	

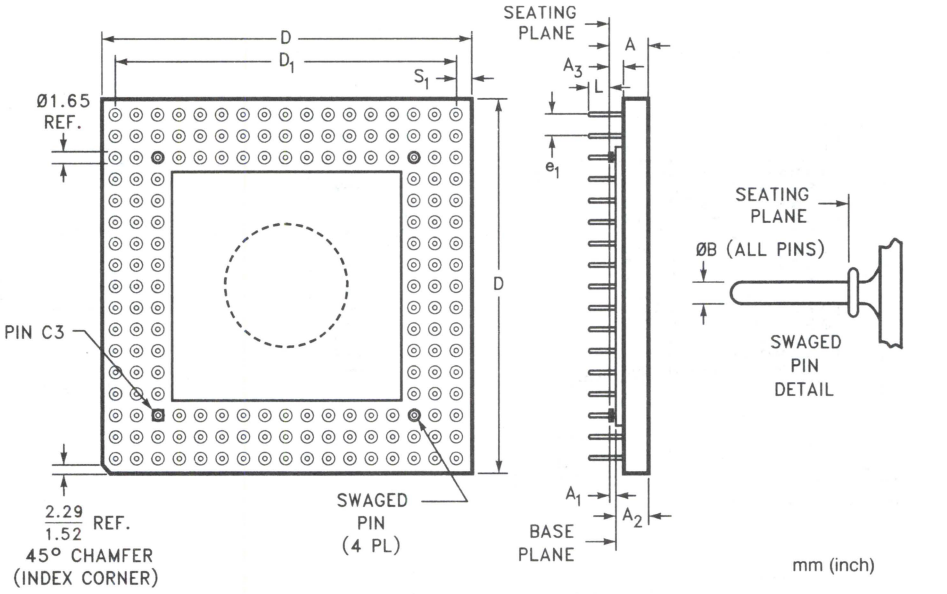
132 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-16

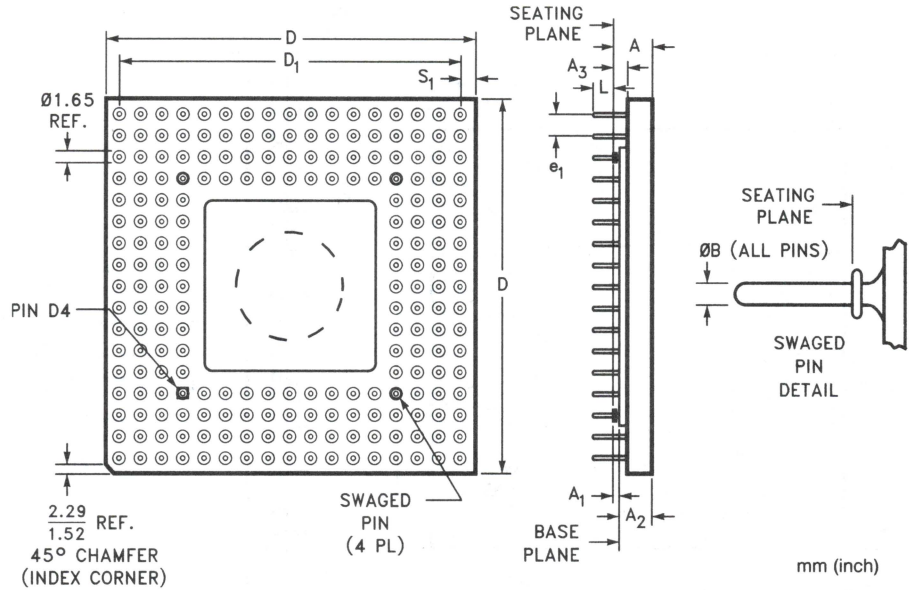
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.57	37.59		1.440	1.480	
D_1	32.89	33.15		1.295	1.305	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S_1	1.27	2.54		0.050	0.100	

168 LEAD CERAMIC PIN GRID ARRAY PACKAGE



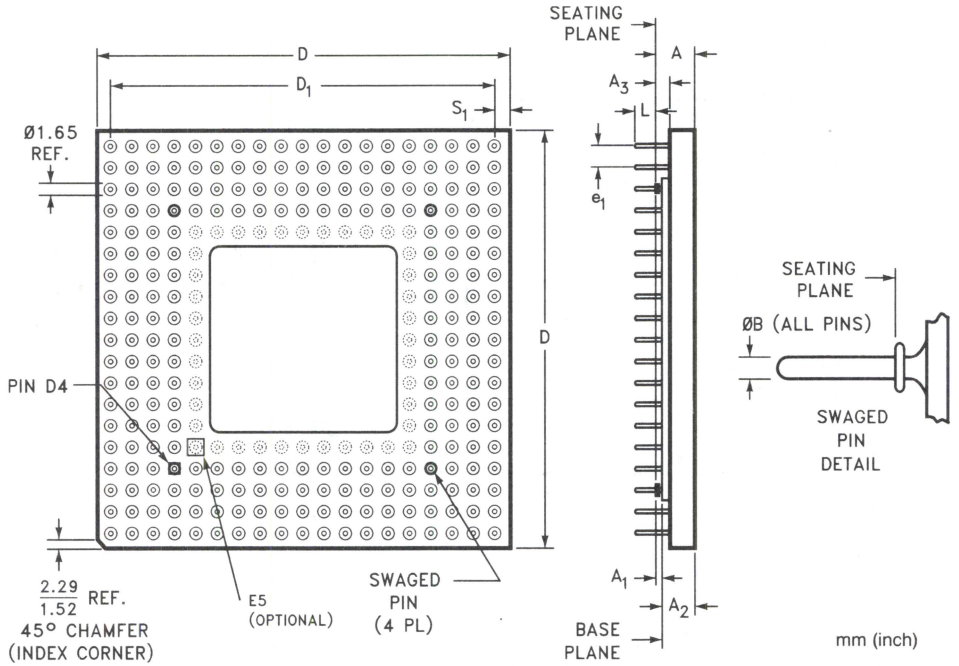
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A_2	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.19	45.21		1.740	1.780	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N		168			168	
S_1	1.52	2.54		0.060	0.100	

208 LEAD CERAMIC PIN GRID ARRAY PACKAGE



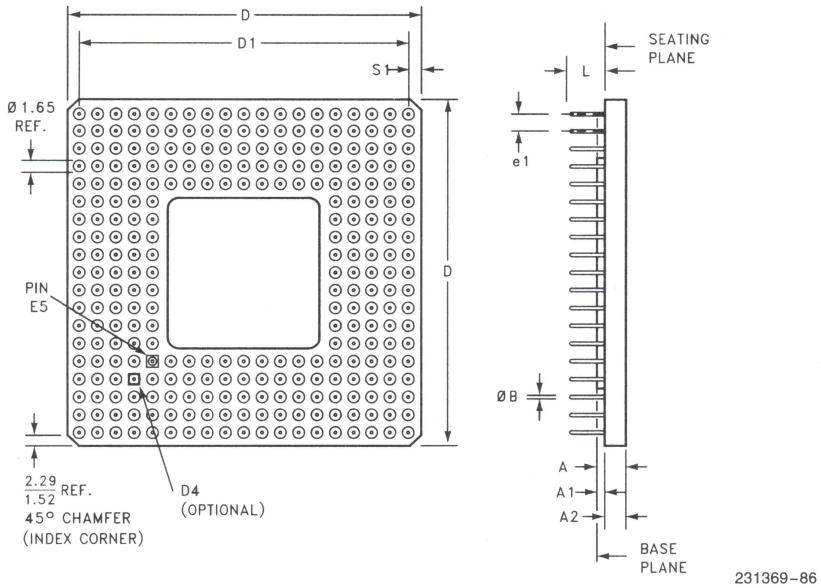
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A_2	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.19	45.21		1.740	1.780	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	208			208		
S_1	1.52	2.54		0.060	0.100	

1.95" SQ CERAMIC PIN GRID ARRAY PACKAGE



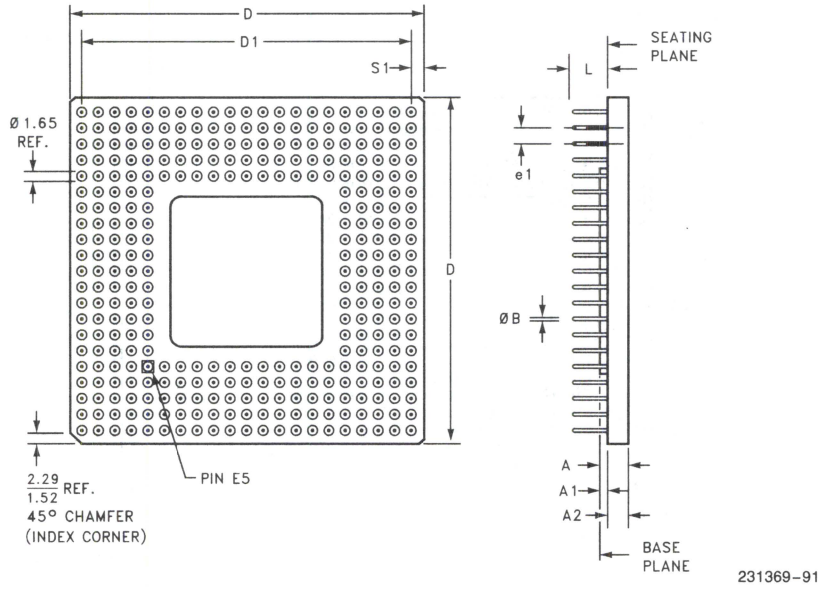
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A_2	2.79	3.56	Solid Lid	0.110	0.140	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	49.27	50.29		1.940	1.980	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	240	280		240	280	
S_1	1.52	2.54		0.060	0.100	

1.95″ SQ CERAMIC PIN GRID ARRAY PACKAGE VARIATION: WITHOUT STAND-OFF PINS



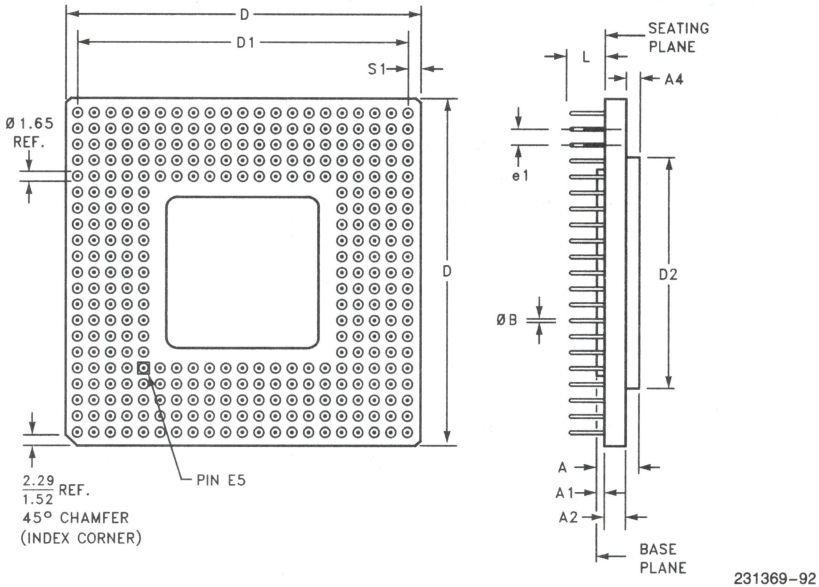
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.84	3.51	Solid Lid	0.112	0.138	Solid Lid
A_1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A_2	2.51	3.07		0.099	0.121	
B	0.43	0.51		0.017	0.020	
D	49.53	50.29		1.940	1.980	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.120	0.130	
N	240	280		240	280	
S_1	1.52	2.54		0.060	0.100	

2.16″ SQ CERAMIC PIN GRID ARRAY PACKAGE VARIATION: WITHOUT STAND-OFF PINS



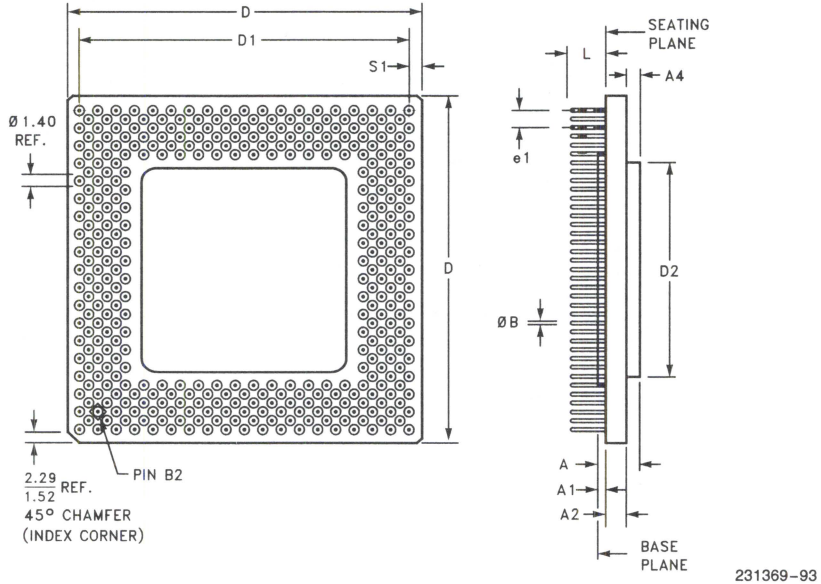
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.94	3.48	Solid Lid	0.116	0.137	Solid Lid
A_1	0.38	0.43	Solid Lid	0.015	0.017	Solid Lid
A_2	2.62	0.43		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	54.61	55.12		2.150	2.170	
D_1	50.67	50.93		1.995	2.005	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.120	0.130	
N	272	320		272	320	
S_1	1.651	2.16		0.065	0.085	

2.16″ SQ CERAMIC PIN GRID ARRAY PACKAGE VARIATION: WITHOUT STAND-OFF PINS, WITH HEAT SPREADER



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.91	4.70	Solid Lid	0.154	0.185	Solid Lid
A_1	0.38	0.43	Solid Lid	0.015	0.017	Solid Lid
A_2	2.62	2.97		0.103	0.117	
A_4	0.97	1.22		0.038	0.048	
B	0.43	0.51		0.017	0.020	
D	54.61	55.12		2.150	2.170	
D_1	50.67	50.93		1.995	2.005	
D_2	37.85	38.35		1.490	1.510	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	272	320		272	320	
S_1	1.651	2.16		0.065	0.085	

1.95″ SQ CERAMIC PIN GRID ARRAY PACKAGE VARIATION: WITHOUT STAND-OFF PINS, STAGGERED 0.100″ PITCH WITH HEAT SPREADER



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.91	4.70	Solid Lid	0.154	0.185	Solid Lid
A_1	0.38	0.43	Solid Lid	0.015	0.017	Solid Lid
A_2	2.62	2.97		0.103	0.117	
A_4	0.97	1.22		0.038	0.048	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
D_2	31.50	32.00		1.240	1.260	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	264	372		264	372	
S_1	1.52	2.54		0.060	0.100	

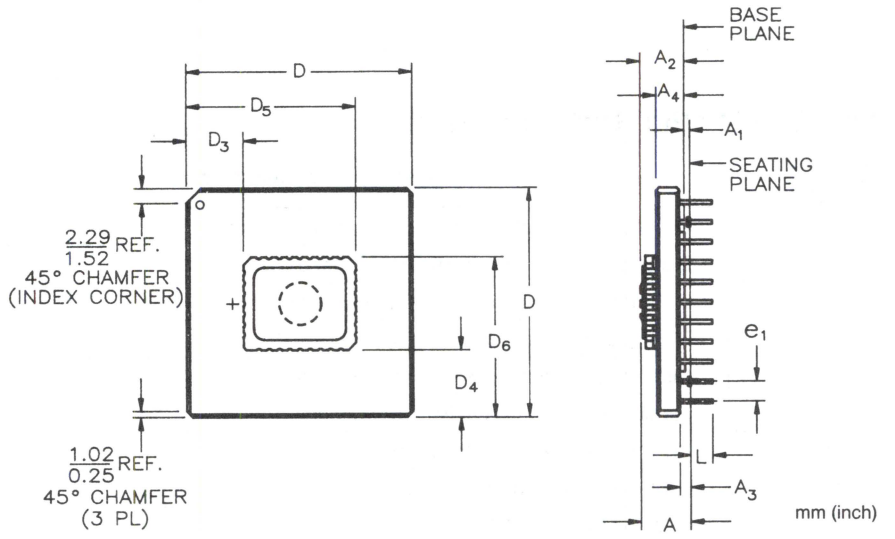
CERAMIC PIN GRID ARRAY MODULE

Symbol List for Pin Grid Array Module

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
A_3	PGA body thickness including lid
A_4	Distance from seating plane to base of body
D	Largest overall package dimension of length
D_3	PGA to LCC start (LCC long dim)
D_4	PGA to LCC start (LCC short dim)
D_5	PGA to LCC end (LCC long dim)
D_6	PGA to LCC end (LCC short dim)
e_1	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.

68 LEAD CERAMIC PIN GRID ARRAY MODULE



Family: Ceramic Pin Grid Array Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	6.10	7.62		0.240	0.300	
A_1	0.64	1.19		0.025	0.047	
A_2	5.21	6.60		0.205	0.260	
A_3	1.14	1.40		0.045	0.055	
A_4	2.72	3.56		0.107	0.140	
D	28.83	29.59		1.135	1.165	
D_3	6.35	8.64		0.250	0.340	
D_4	7.37	9.40		0.290	0.370	
D_5	20.07	23.62		0.790	0.930	
D_6	18.54	22.61		0.730	0.890	
e_1	2.29	2.79		0.090	0.110	
L	2.41	3.18		0.095	0.125	
N	68 PGA			68 PGA		
N	32 LCC			32 LCC		

CERAMIC QUADPACK PACKAGE

Symbol List for Ceramic Quadpack Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A_1	Ceramic body thickness
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_1	Largest overall package dimension of length excluding leads
D_2	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between centerlines of terminal leads
L	Lead dimension free lead length
S	Distance from true position centerline of end lead position to the extremity of the body
S_1	Linear spacing of true maximum lead position from lead edge to package edge

NOTES:
Controlling dimension: millimeter.
Dimension "e_1" ("e") is non-cumulative.
Pin numbering is ascending in the counterclockwise direction.
Dimensions "B", "B_1" and "C" are nominal.

Packaging Family Attributes	
Category	Ceramic Quadpack
Acronym	CQFP
Lead Configuration	Quad
Lead Counts	68
Lead Finish	Gold Plate or SolderCoat
Lead Pitch	0.050″
Board Assembly Type	Socket and Surface Mount

NOTES:
1. Alloy 42 or Kovar Leads.
2. Sold unformed in carrier.

68 LEAD CERAMIC QUADPACK PACKAGE

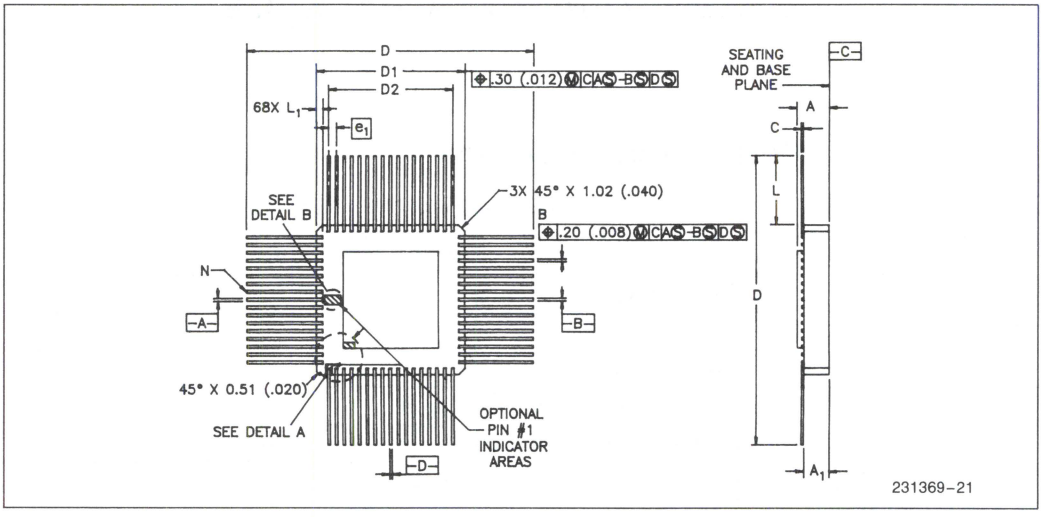


Figure 1. Principle Dimensions and Datums

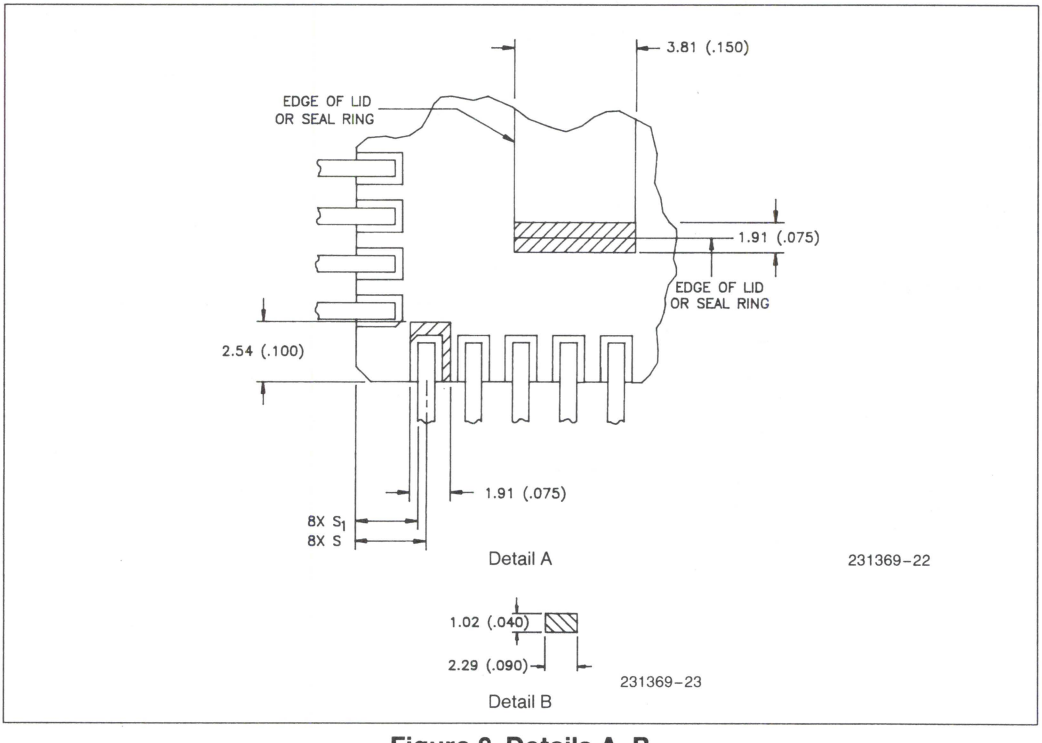


Figure 2. Details A, B

CERAMIC QUADPACK PACKAGE

Family: 68 Lead Ceramic Quadpack Family						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.69	Solid Lid	0.088	0.106	Solid Lid
A	2.91	3.68	EPROM Lid	0.115	0.145	EPROM Lid
A_1	1.98	2.39		0.078	0.094	
B	0.41	0.53	68 Places	0.016	0.021	68 Places
B_1	1.02	1.52	Typical	0.040	0.060	Typical
B_2	0.76	1.02	Typical	0.030	0.040	Typical
B_3	0.13	0.51	Typical	0.005	0.020	Typical
C	0.20	0.31		0.008	0.012	
D	41.66	47.50		1.640	1.870	
D_1	23.52	24.64		0.926	0.970	
D_2	20.32		BSC	0.800		BSC
e_1	1.27 BSC		64 Places	0.050 BSC		64 Places
L	8.89	11.43		0.350	0.450	
L_1	1.02	1.52		0.040	0.060	
N	68			68		
S	1.91		REF	0.075		REF
S_1	1.27			0.050		

CERAMIC QUAD FLATPACK PACKAGE

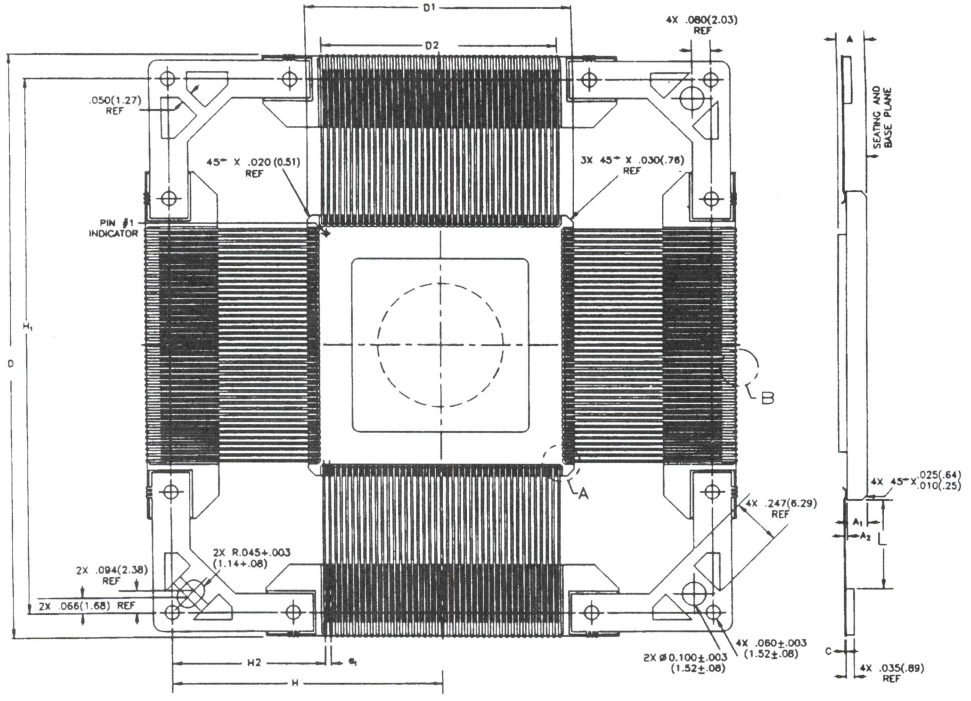
Symbol List for Quadpack Family

Letter or Symbol	Description of Dimensions
A	Distance from Seating Plane to Highest Point of Body (Lid)
A_1	Ceramic Body Thickness
A_2	Distance from Top of Ceramic to Bottom of Lead
B	Width of Terminal Leads
C	Thickness of Terminal Leads
D	Largest Overall Package Dimension of Length
D_1	Largest Overall Package Dimension of Length Excluding Leads
D_2	A Body Length Dimension, Outer Lead Center to Outer Lead Center
e_1	Linear Spacing between Centerlines of Terminal Leads
H	Distance from Body Centerline to Locator Holes
H_1	Distance between Opposite Locator Holes
H_2	Distance from End Lead Centerline to Locator Holes
L	Lead Dimension Free Lead Length
S	Distance from True Position Centerline of End Lead Position to the Extremity of the Body
S_1	Linear Spacing of True Maximum Lead Position from Lead Edge to Package Edge

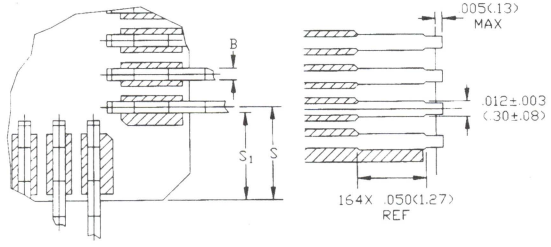
NOTES:
1. Dimension "e_1" ("e") is non-cumulative.
2. Pin numbering is ascending in the counterclockwise direction.

Packaging Family Attributes	
Category	Ceramic Quad Flatpack
Acronym	CQFP
Lead Configuration	Quad
Lead Counts	164, 196
Lead Finish	Gold Plate, 60 Microinches of Gold over 100–350 Microinches of Nickel Plate
Lead Material	Kovar
Lead Braze Material	Copper/Silver Eutectic
Lead Pitch	0.025″
Board Assembly Type	Socket and Surface Mount

164 LEAD CERAMIC QUAD FLATPACK PACKAGE
VARIATION: CAVITY UP WITH N/C TIE BAR



231369-24



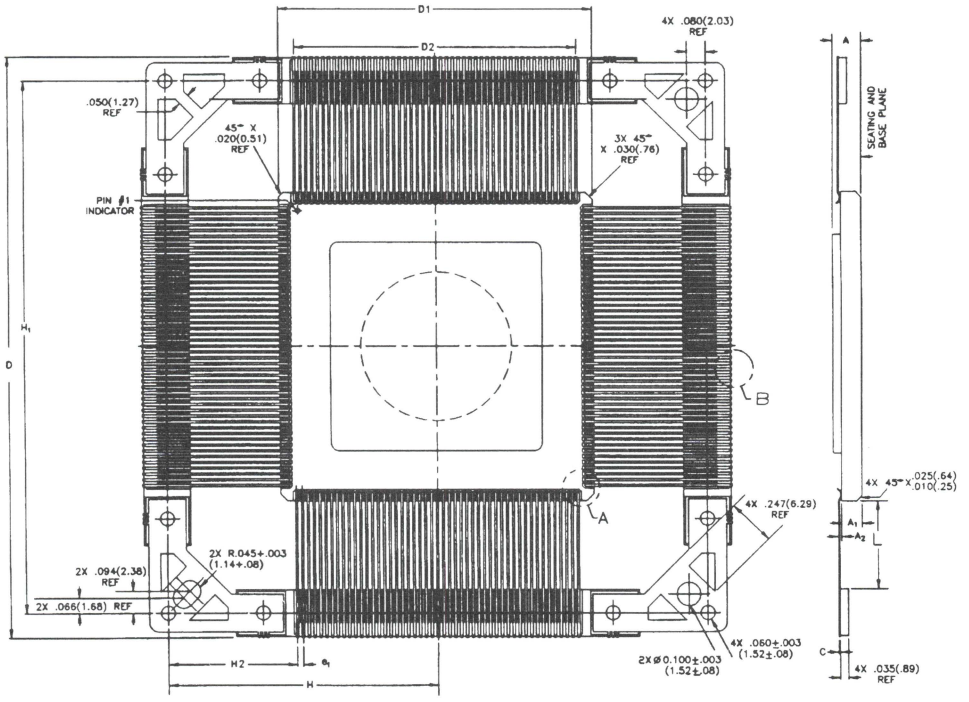
DETAIL A DETAIL B

231369-25

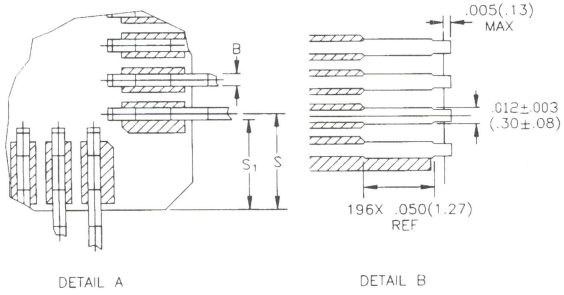
164 LEAD CERAMIC QUAD FLATPACK PACKAGE VARIATION: CAVITY UP WITH N/C TIE BAR (Continued)

Family: Ceramic Quadpack						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A_1	1.98	2.39		0.078	0.094	
A_2	0.15	0.30		0.006	0.012	
B	0.18	0.25		0.007	0.010	
C	0.10	0.15		0.004	0.006	
D	63.50	64.01		2.500	2.520	
D_1	28.45	28.96		1.120	1.140	
D_2	25.40		Basic	1.000		Basic
e_1	0.58	0.69		0.023	0.027	
H	29.21		Basic	1.150		Basic
H_1	58.42		Basic	2.30		Basic
H_2	16.51		Basic	0.650		Basic
L	9.27	10.03		0.365	0.395	
N	164			164		
S	1.52	2.03	Reference	0.060	0.080	Reference
S_1	1.52	1.93		0.060	0.076	

196 LEAD CERAMIC QUAD FLATPACK PACKAGE VARIATION: CAVITY UP WITH N/C TIE BAR



231369-26



231369-27

196 LEAD CERAMIC QUADPACK PACKAGE VARIATION: CAVITY UP WITH N/C TIE BAR (Continued)

Family: Ceramic Quadpack						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A_1	1.96	2.39		0.078	0.094	
A_2	0.15	0.30		0.006	0.012	
B	0.20	0.25		0.008	0.010	
C	0.10	0.20		0.004	0.008	
D	63.50	64.01		2.500	2.520	
D_1	33.65	34.16		1.325	1.345	
D_2	30.48		Basic	1.200		Basic
e_1	0.58	0.69		0.023	0.027	
H	29.21		Basic	1.150		Basic
H_1	58.42		Basic	2.30		Basic
H_2	19.05		Basic	0.750		Basic
L	9.27	10.03		0.365	0.395	
N	196			196		
S	1.27	2.03	Reference	0.050	0.080	Reference
S_1	1.14	1.93		0.045	0.076	

NOTE:
1. Currently for Military application only.

CERDIP DUAL IN-LINE PACKAGE

Symbol List for Cerdip Dual In-Line Family

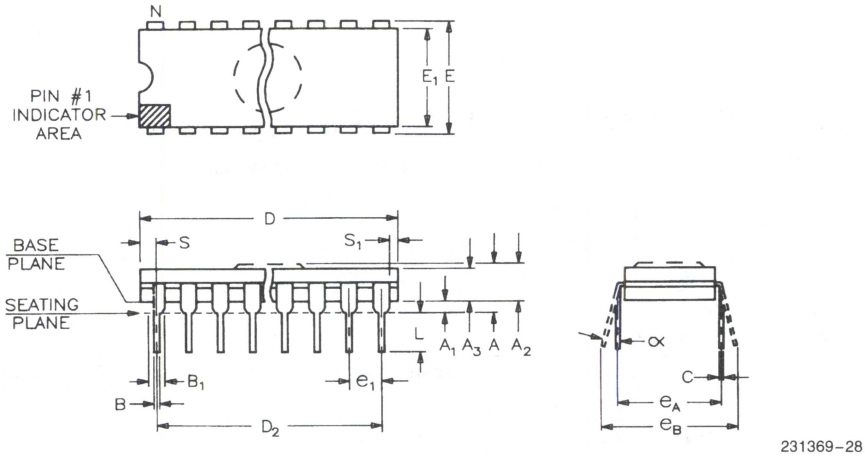
Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_2	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E_1	Body width dimensions not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B_1" is nominal.

Packaging Family Attributes	
Category	Cerdip
Acronym	Cerdip
Lead Configuration	Dual-In-Line
Lead Counts	16, 18, 20, 22, 24, 32, 40, 44
Lead Finish	Tin Plate of SolderPlate
Lead Pitch	0.100″
Board Assembly Type	Socket and Surface Mount

NOTES:
1. Alloy 42 Leads.
2. Pressed Ceramic Body.
3. UV Window available for reprogramming.

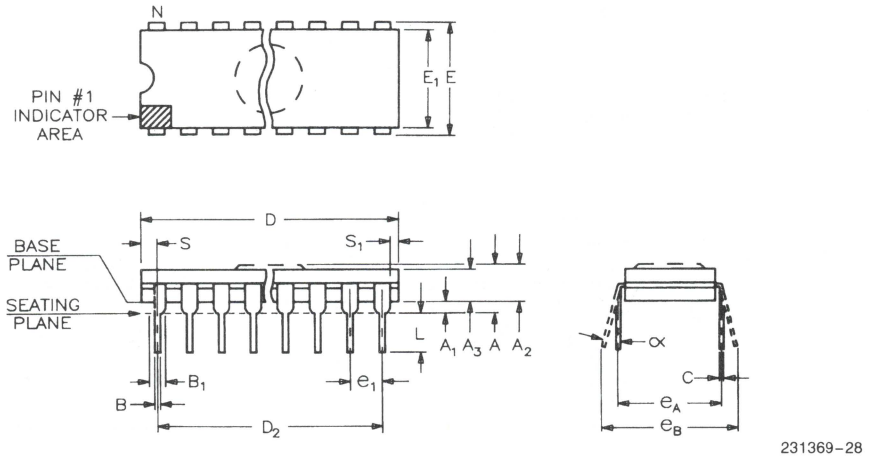
16 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.44		0.140	0.175	
A_3	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	19.05	19.94		0.750	0.785	
D_2	17.78		Reference	0.700		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.90		0.280	0.311	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	16		½ Leads	16		½ Leads
S	0.25	1.27		0.010	0.050	
S_1	0.13			0.005		

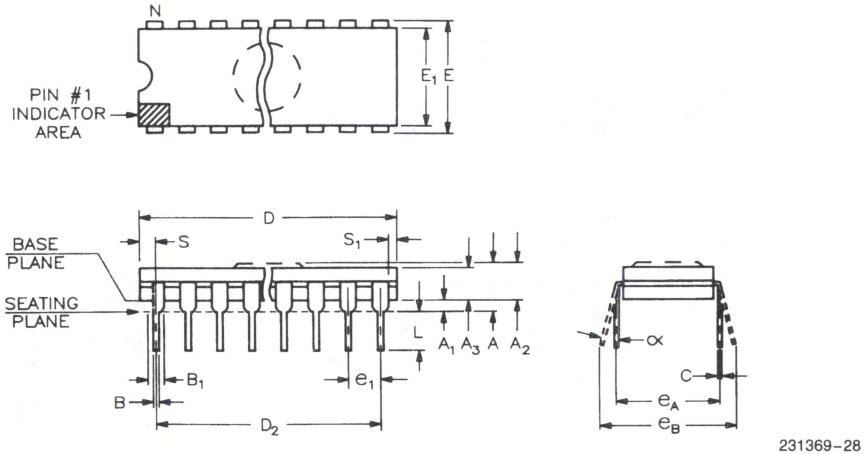
18 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.44		0.140	0.175	
A_3	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.35	23.24		0.880	0.915	
D_2	20.32		Reference	0.800		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.90		0.280	0.311	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	18		½ Leads	18		½ Leads
S	0.64	1.78		0.025	0.070	
S_1	0.13			0.005		

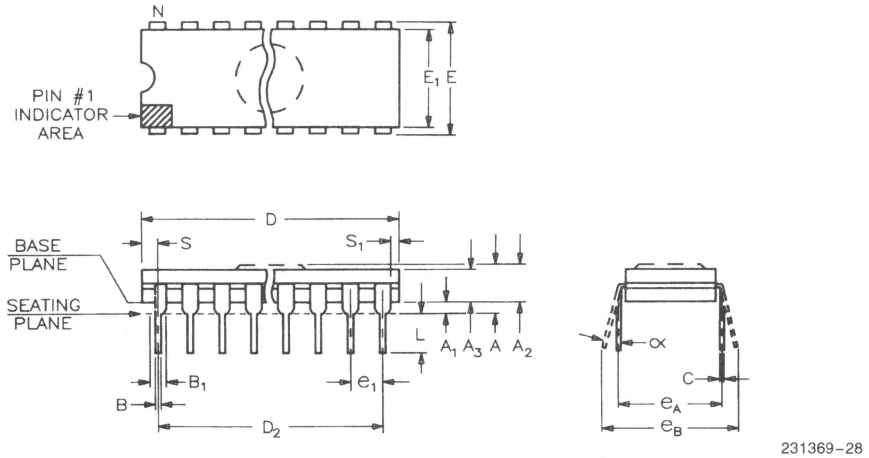
20 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.24		0.140	0.167	
A_3	3.56	4.24		0.140	0.167	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	24.38	25.27		0.960	0.995	
D_2	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.90		0.280	0.311	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	20		½ Leads	20		½ Leads
S	0.38	1.78		0.015	0.070	
S_1	0.13			0.005		

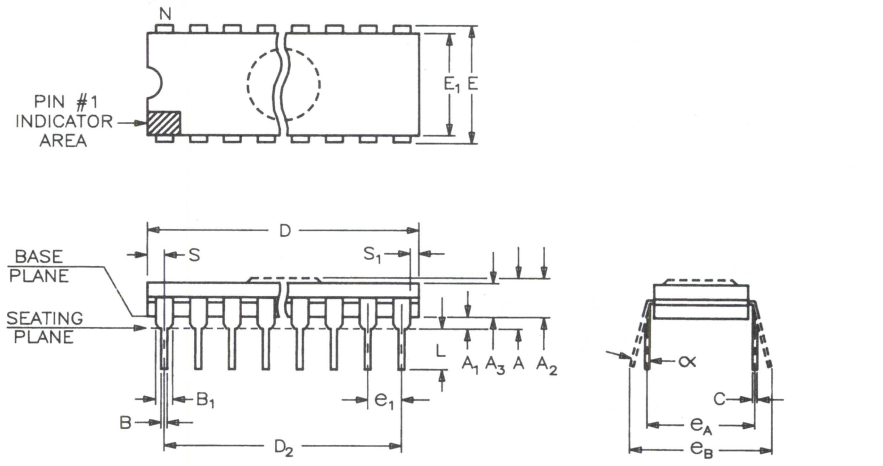
22 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.81	4.57		0.150	0.180	
A_3	3.81	4.57		0.150	0.180	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	26.92	27.81		1.060	1.095	
D_2	25.40		Reference	1.000		Reference
E	10.16	10.67		0.400	0.420	
E_1	9.53	10.29		0.375	0.405	
e_1	2.29	2.79		0.090	0.110	
e_A	10.41		Reference	0.410		Reference
e_B	10.67	12.70		0.420	0.500	
L	3.18	3.81		0.125	0.150	
N	22		½ Leads/400 MIL	22		½ Leads/400 MIL
S	0.38	1.52		0.015	0.060	
S_1	0.13			0.005		

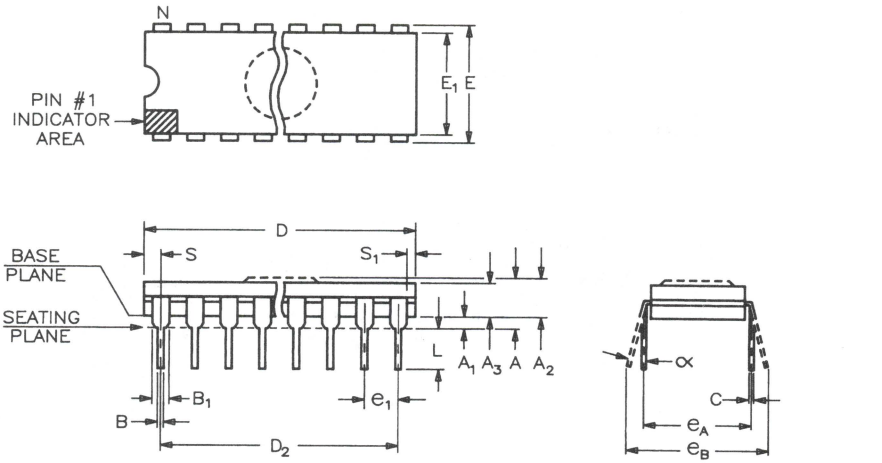
24 LEAD CERDIP DUAL IN-LINE PACKAGE (300 MIL)



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.83		0.140	0.190	
A_3	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	Typical
B_1	1.42		Typical	0.056		Typical
C	0.23	0.30	Typical	0.009	0.012	
D	31.50	32.64		1.240	1.285	
D_2	27.94		Reference	1.100		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.87		0.280	0.310	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	4.06		0.125	0.160	
N	24		300 MIL	24		300 MIL
S		2.29			0.090	
S_1	0.13			0.005		

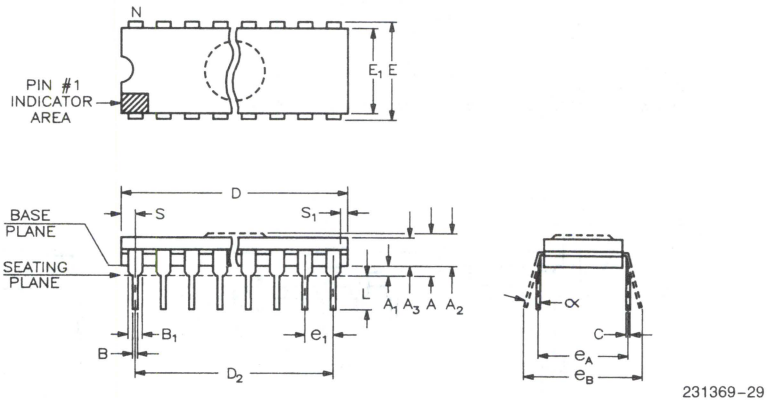
24 LEAD CERDIP DUAL IN-LINE PACKAGE (600 MIL)



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.70		0.140	0.185	
A_3	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	31.50	32.64		1.240	1.285	
D_2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E_1	13.08	15.24		0.515	0.600	
e_1	2.29	2.79		0.090	0.110	
e_A	15.49		Reference	0.610		Reference
e_B	15.75	17.78		0.620	0.700	
L	3.18	3.81		0.125	0.150	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S_1	0.13			0.005		

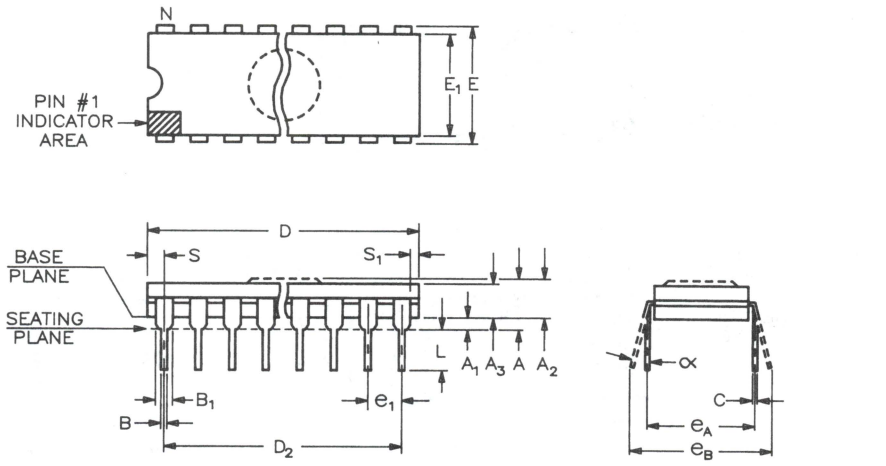
28 LEAD CERDIP DUAL IN-LINE PACKAGE (300 MIL) VARIATION: SKINNY DIP



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.83		0.140	0.190	
A_3	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	Typical
B_1	1.42		Typical	0.056		Typical
C	0.23	0.30	Typical	0.009	0.012	
D	36.58	37.72		1.440	1.485	
D_2	33.02		Reference	1.300		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.87		0.280	0.310	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	4.06		0.125	0.160	
N	28		300 MIL	28		300 MIL
S		2.29			0.090	
S_1	0.13			0.005		

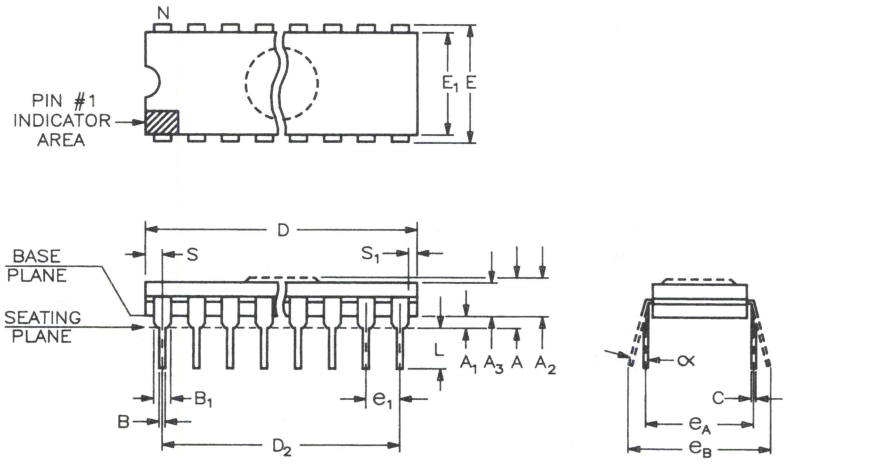
28 LEAD CERDIP DUAL IN-LINE PACKAGE (600 MIL)



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.95		0.140	0.195	
A_3	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	36.58	37.72		1.440	1.485	
D_2	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E_1	13.08	15.37		0.515	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	15.49		Reference	0.610		Reference
e_B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	28			28		
S	1.40	2.29		0.055	0.090	
S_1	0.13			0.005		

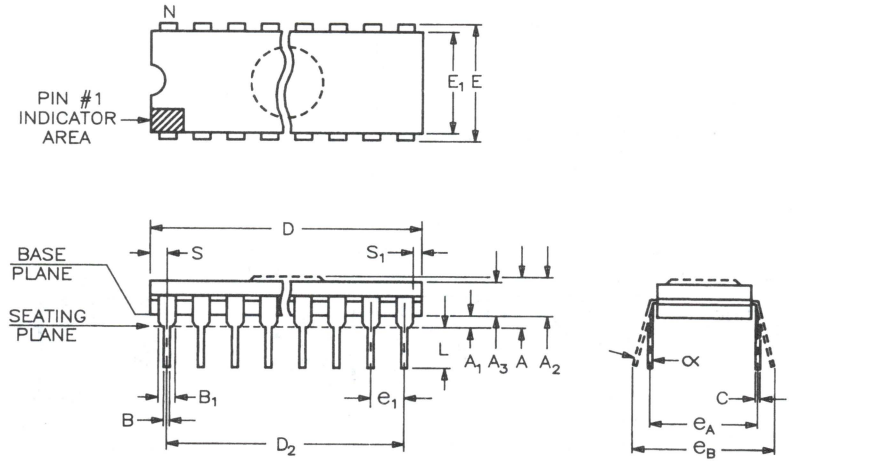
32 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.95		0.140	0.195	
A_3	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	41.66	42.67		1.640	1.680	
D_2	41.91		Reference	1.650		Reference
E	15.24	15.75		0.600	0.620	
E_1	14.48	15.37		0.570	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	15.49		Reference	0.610		Reference
e_B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	32			32		
S	1.40	2.29		0.055	0.090	
S_1	0.13			0.005		

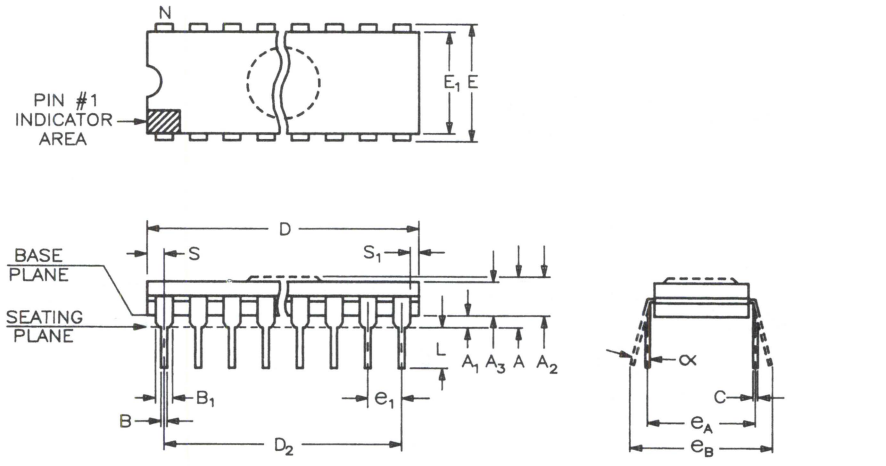
40 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.95		0.140	0.195	
A_3	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	51.69	52.96		2.035	2.085	
D_2	48.26		Reference	1.900		Reference
E	15.24	15.75		0.600	0.620	
E_1	13.08	15.37		0.515	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	15.49		Reference	0.610		Reference
e_B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	40			40		
S	1.40	2.29		0.055	0.090	
S_1	0.13			0.005		

42 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A_1	0.38			0.015		
A_2	3.56	4.95		0.140	0.195	
A_3	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	54.23	55.50		2.135	2.185	
D_2	50.80		Reference	2.000		Reference
E	15.24	15.75		0.600	0.620	
E_1	13.08	15.37		0.515	0.605	
e_1	2.29	2.79		0.090	0.110	
e_A	15.49		Reference	0.610		Reference
e_B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	42			42		
S	1.40	2.29		0.055	0.090	
S_1	0.13			0.005		

CERQUAD PACKAGE

Symbol List for Cerquad Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Shoulder to Board Height
C	Lead Thickness
CP	Seating Plane Coplanarity
D	Outside Dimension
D_1	Ceramic Body Dimension
D_2	Footprint
D_3	Footprint
E	Outside Dimension
E_1	Ceramic Body Dimension
E_2	Footprint
E_3	Footprint
N	No. of Leads

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. To be determined at seating plane —E—.
3. Dimensions D1 and E1 do not include glass protrusion.
4. Controlling dimension, inch.
5. All dimensions and tolerances include lead trim offset and lead plating finish.

Packaging Family Attributes	
Category	Cerquad
Acronym	Cerquad
Lead Configuration	Quad
Lead Counts	44, 52, 68
Lead Finish	SolderCoat
Lead Pitch	0.050″
Board Assembly Type	Socket

NOTES:
1. Alloy 42 - "J" Leads.
2. Pressed Ceramic Body.
3. UV Window available for reprogramming.
4. Compatible with PLCC Footprint.
5. Not certified for Surface Mount, must be Socketed.

CERQUAD PACKAGE (SQUARE)

Family: 44 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	3.94	4.57	0.155	0.180		
A_1	2.29	3.05	0.090	0.120	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	17.40	17.65	0.685	0.695	0.690	
D_1	16.00	16.66	0.630	0.656	0.650	(Note 3)
D_2	15.24	15.75	0.590	0.630	0.620	(Note 2)
D_3	12.70		0.500			Reference
E	17.40	17.65	0.685	0.695	0.690	
E_1	16.36	16.66	0.635	0.656	0.650	(Note 3)
E_2	15.24	15.75	0.590	0.630	0.620	(Note 2)
E_3	12.70		0.500			Reference
N	44		44			

CERQUAD PACKAGE (SQUARE)

Family: 52 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	4.20	4.83	0.165	0.190		
A_1	2.29	3.30	0.090	0.130	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	19.94	20.19	0.785	0.795	0.790	
D_1	18.542	19.202	0.730	0.756	0.750	(Note 3)
D_2	17.53	18.54	0.690	0.730	0.720	(Note 2)
D_3	15.24		0.600			Reference
E	19.94	20.19	0.785	0.795	0.790	
E_1	18.669	19.202	0.735	0.756	0.750	(Note 3)
E_2	17.53	18.54	0.690	0.730	0.720	(Note 2)
E_3	15.24		0.600			Reference
N	52		52			

Family: 68 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	3.94	4.83	0.155	0.190		
A_1	2.29	3.05	0.090	0.120	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	25.02	25.27	0.985	0.995	0.990	
D_1	23.62	24.33	0.930	0.958	0.950	(Note 3)
D_2	22.86	23.37	0.890	0.930	0.920	(Note 2)
D_3	20.32		0.800			Reference
E	25.02	25.27	0.985	0.995	0.990	
E_1	23.93	24.33	0.935	0.958	0.950	(Note 3)
E_2	22.86	23.37	0.890	0.930	0.920	(Note 2)
E_3	20.32		0.800			Reference
N	68		68			

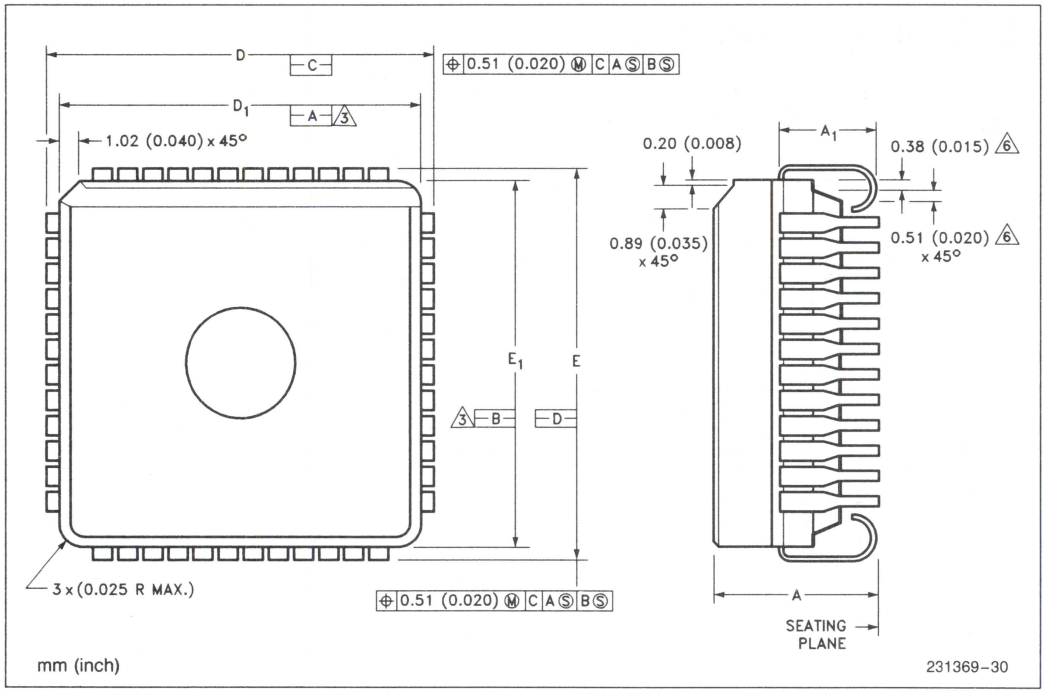


Figure 1. Principal Dimensions and Datums

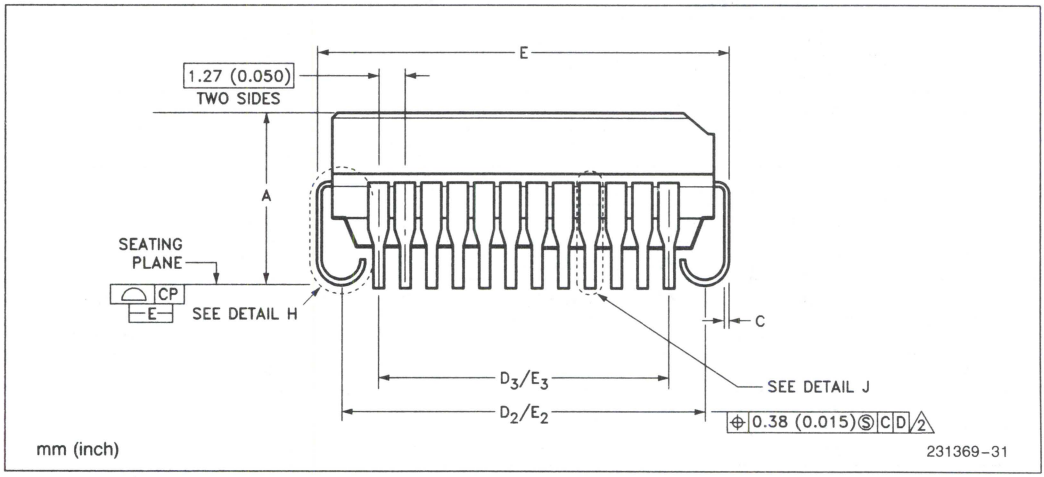
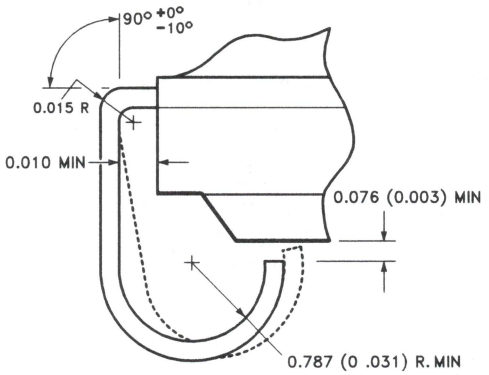


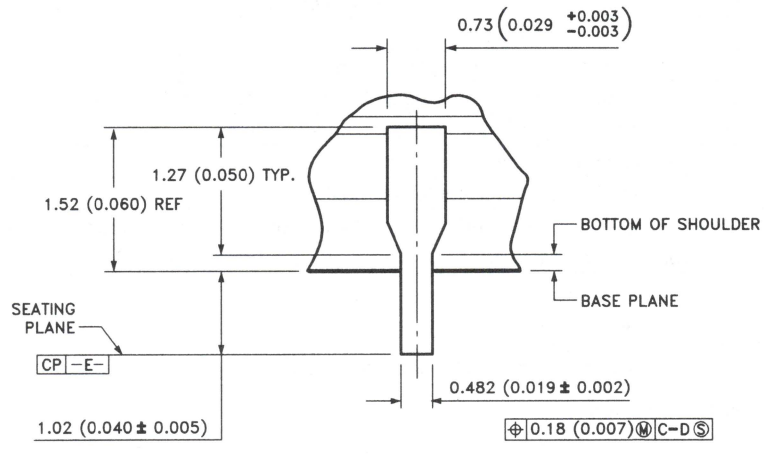
Figure 2. Terminal Details



mm (inch)

231369-32

Detail H



mm (inch)

231369-33

Detail J
Typ All Sides

PLASTIC DUAL IN-LINE PACKAGE

Symbol List for Plastic Dual In-Line Family

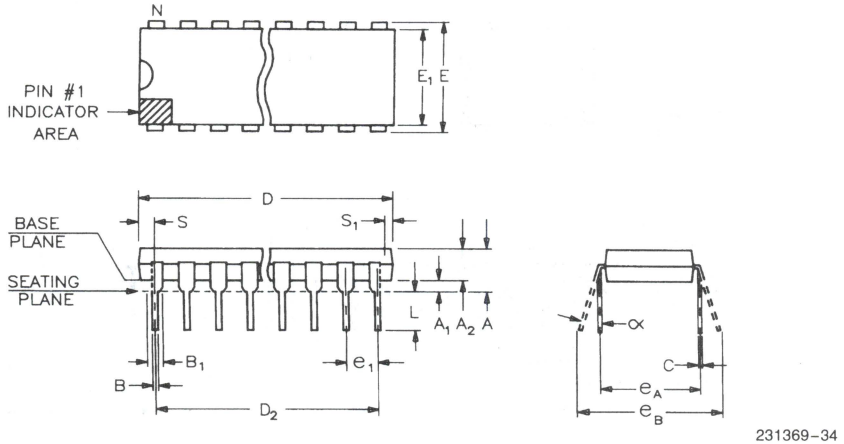
Letter or Symbol	Description of Dimensions
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane
A	Distance from seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locates seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_2	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E_1	Body width dimensions not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B_1" is nominal.
5. Details of Pin 1 identifier are optional.

Packaging Family Attributes	
Category	Plastic Dual-In-Line
Acronym	PDIP
Lead Configuration	Dual-In-Line
Lead Counts	16, 18, 20, 24, 28, 32, 40, 48, 64
Lead Finish	SolderCoat
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount

NOTES:
1. Alloy 42 and Cu Alloy Leads.
2. Novalac Body.

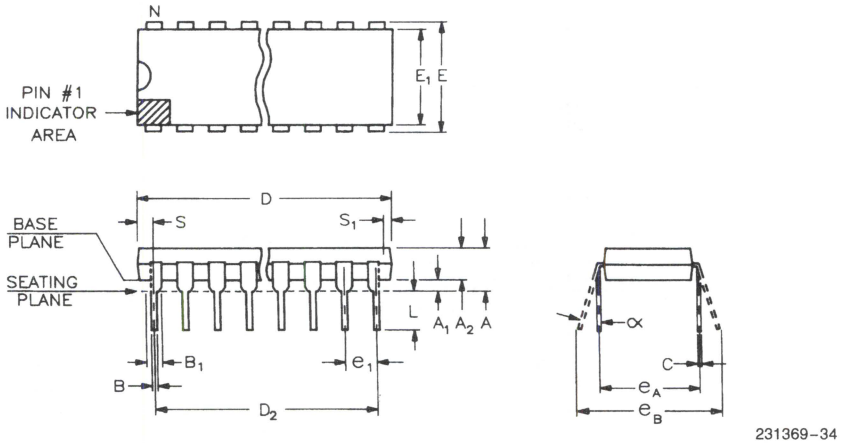
16 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: ½ LEAD



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.18	3.56		0.125	0.140	
B	0.41	0.53		0.016	0.021	
B_1	1.52		Typical	0.060		Typical
C	0.20	0.36	Typical	0.008	0.014	Typical
D	18.78	19.81		0.74	0.780	
D_2	17.78		Reference	0.700		Reference
E		8.13			0.320	
E_1	6.10	6.60		0.240	0.260	
e_1	2.29	2.79	Typical	0.090	0.110	Typical
e_A	7.37		Reference	0.290		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	16		1/2 Lead	16		1/2 Lead
S	0.51	1.02		0.020	0.040	
S_1	0.23			0.009		

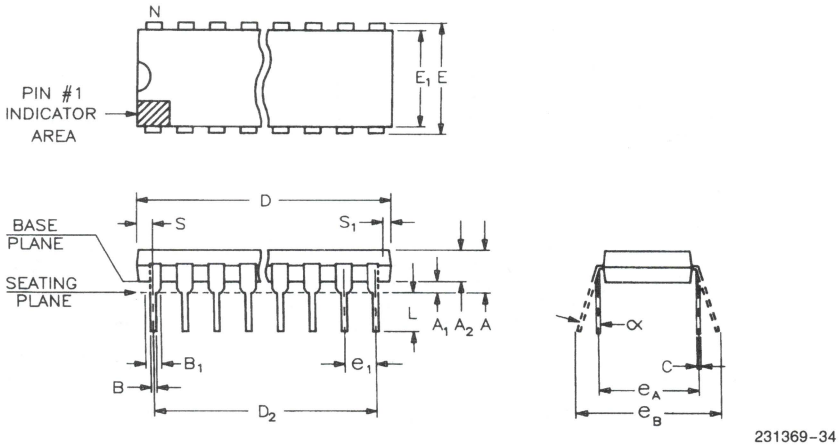
16 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: ½ LEAD/WIDEBODY



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.18	3.61		0.125	0.142	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	19.18	19.81		0.755	0.780	
D_2	17.78		Reference	0.700		Reference
E		8.13			0.320	
E_1	6.73	6.99		0.265	0.275	
e_1	2.29			0.090	0.110	
e_A	7.37		Reference	0.290		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	16		½ Lead/Widebody	16		½ Lead/Widebody
S	0.51	1.02		0.020	0.040	
S_1	0.23			0.009		

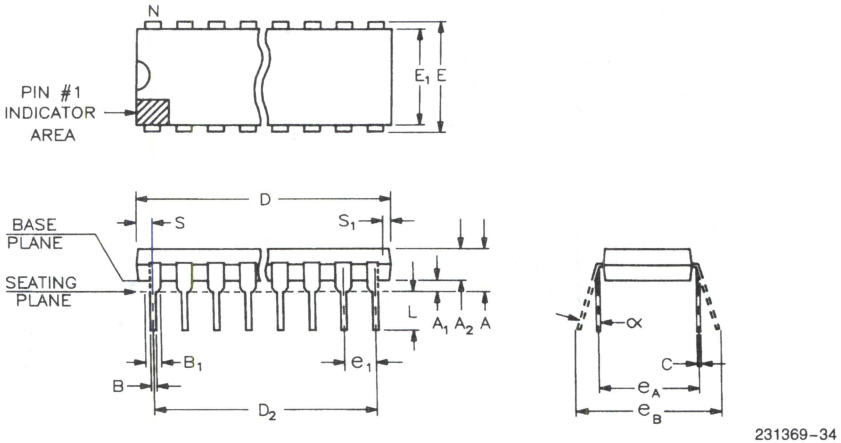
18 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: ½ LEAD



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.57	4.57		0.140	0.180	
A_1	0.51			0.020		
A_2	3.06	4.06		0.120	0.160	
B	0.36	0.56		0.014	0.022	
B_1	1.27		Typical	0.050		Typical
C	0.20	0.30		0.008	0.012	
D	22.83	23.09		0.899	0.909	
D_2						
E	8.13		Typical	0.320		Typical
E_1	6.27	6.53		0.247	0.257	
e_1	2.54		Typical	0.100		Typical
e_A	7.62		Typical	0.300		Typical
e_B						
L	3.05			0.120		
N	18		½ Lead	18		½ Lead
S						
S_1						

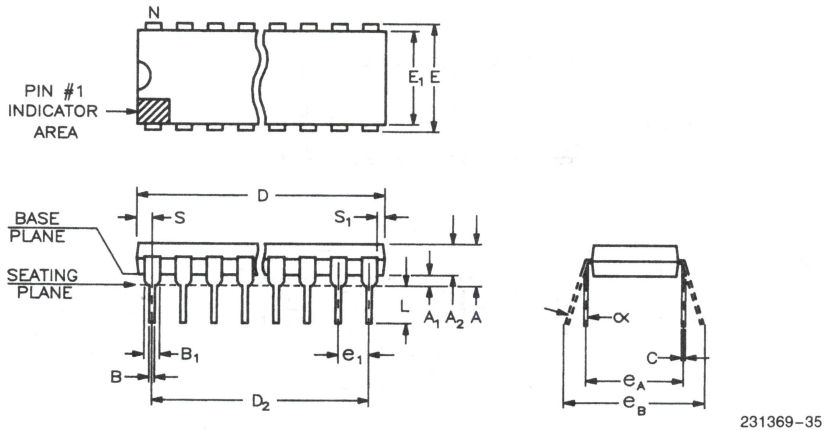
18 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: ½ LEAD/WIDEBODY



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.004			0.197	
A_1	0.51			0.020		
A_2	3.43	3.68		0.135	0.145	
B	0.41	0.58		0.016	0.023	
B_1	1.19	1.49		0.047	0.065	
C	0.20	0.30		0.008	0.012	
D	21.84	22.37		0.860	0.875	
D_2						
E	7.62		Typical	0.300		Typical
E_1		7.37			0.290	
e_1	2.54			0.100		Typical
e_A						
e_B						
L	3.00	3.68		0.118		
N	18		Widebody	18		Widebody
S						
S_1						

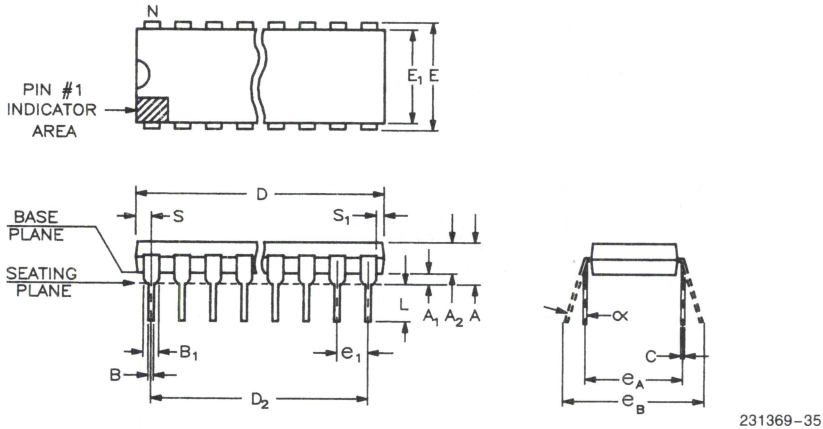
18 LEAD PLASTIC DUAL IN-LINE PACKAGE



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	5°		0°	5°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.18	3.68		0.125	0.145	
B	0.41	0.53		0.016	0.021	
B_1	1.52		Typical	0.060		Typical
C	0.20	0.36	Typical	0.008	0.014	Typical
D	21.34	23.37		0.240	0.920	
D_2	20.32		Reference	0.800		Reference
E		8.26			0.320	
E_1	6.10	7.37		0.240	0.290	
e_1	2.29	2.79		0.090	0.110	
e_A	7.66		Reference	0.290		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	18			18		
S	1.02	1.52		0.040	0.060	
S_1	0.23			0.009		

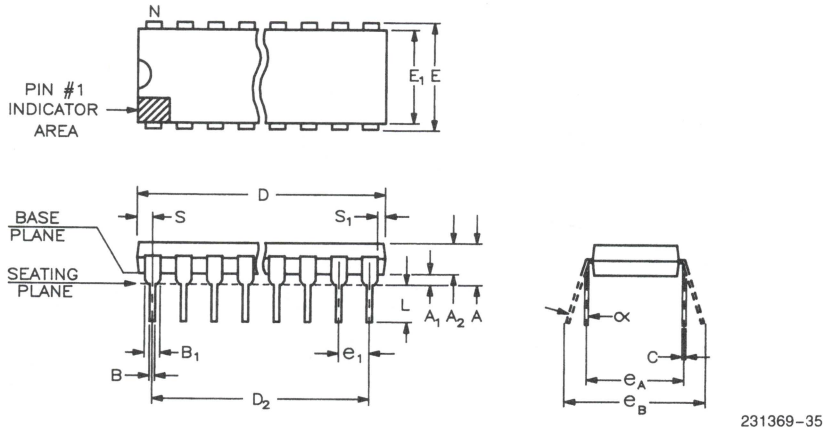
18 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: WIDEBODY



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.18	3.56		0.125	0.140	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.73	23.37		0.895	0.920	
D_2	20.32		Reference	0.800		Reference
E		8.13			0.320	
E_1	6.73	6.98		0.265	0.275	
e_1	2.29	2.79		0.090	0.110	
e_A	7.37		Reference	0.290		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.18	3.68		0.125	0.145	
N	18		Widebody	18		Widebody
S	1.02	1.52		0.040	0.060	
S_1	0.23			0.009		

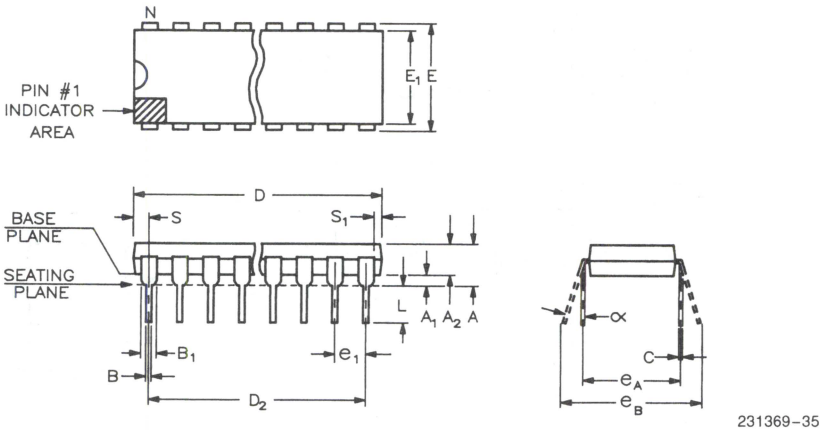
20 LEAD PLASTIC DUAL IN-LINE PACKAGE



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.18	3.68		0.125	0.145	
B	0.41	0.58		0.016	0.023	
B_1	1.19	1.52		0.047	0.060	
C	0.20	0.30		0.008	0.012	
D	24.43	26.67		0.962	1.050	
D_2	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E_1	6.22	6.48		0.245	0.255	
e_1	2.29	2.79		0.090	0.110	
e_A	7.37		Reference	0.290		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.00	3.68		0.118	0.145	
N	20			20		
S	1.40	1.91		0.055	0.075	
S_1	0.61			0.024		

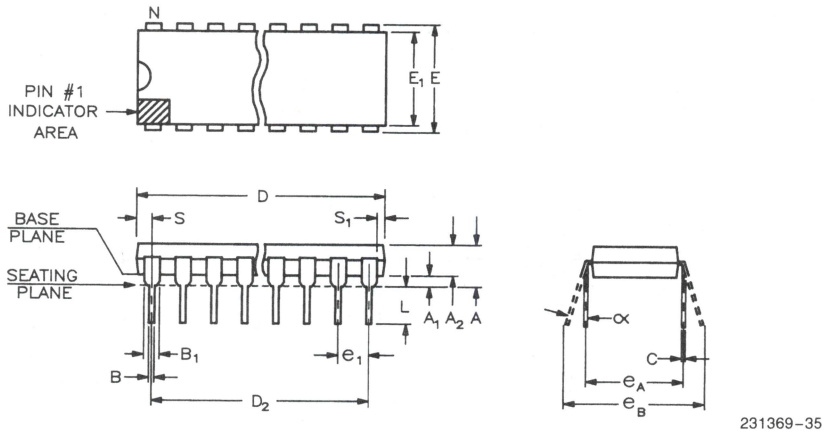
24 LEAD PLASTIC DUAL IN-LINE PACKAGE (300 MIL) VARIATION: SKINNY DIP



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.32			0.170	
A_1	0.38			0.015		
A_2	3.18	3.65		0.130		
B	0.41	0.51		0.016	0.020	
B_1	1.40	1.65		0.055	0.065	
C	0.20	0.30		0.008	0.012	
D	31.34	31.88		1.245	1.255	
D_2	27.94		Reference	1.100		Reference
E	7.62	8.26		0.300	0.325	
E_1	6.35	8.26		0.250	0.325	
e_1	2.54		Reference	0.100		Reference
e_A	7.62		Reference	0.300		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	24		300 MIL	24		300 MIL
S	1.78	2.03		0.070	0.080	
S_1	1.02			0.040		

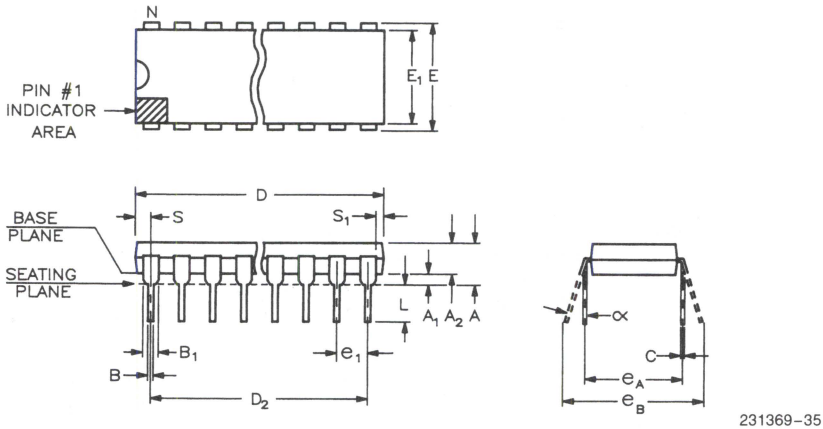
24 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.68	4.06		0.145	0.160	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	31.37	32.00		1.235	1.260	
D_2	27.94		Reference	1.100		Reference
E		15.75			0.620	
E_1	13.59	13.84		0.535	0.545	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	24		600 MIL	24		600 MIL
S	1.52	2.03		0.060	0.080	
S_1	0.74			0.029		

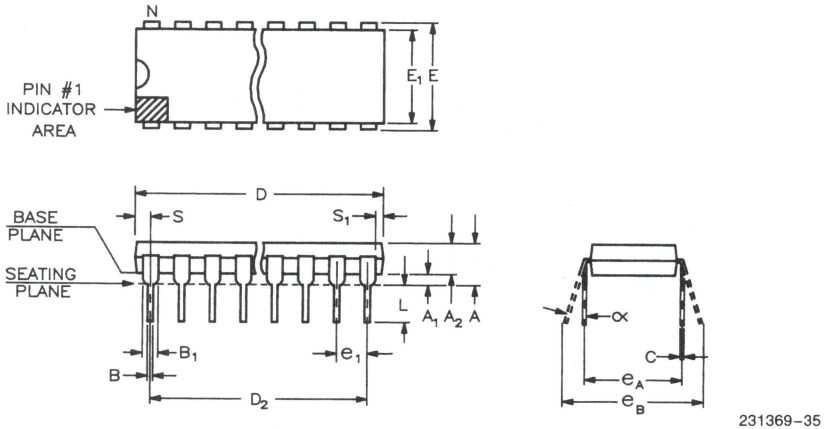
28 LEAD PLASTIC DUAL IN-LINE PACKAGE (300 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.32			0.170	
A_1	0.38			0.015		
A_2	3.30		Typical	0.130		Typical
B	0.41	0.51		0.016	0.020	
B_1	1.14	1.40		0.045	0.055	
C	0.20	0.30		0.008	0.012	
D	34.16	34.42		1.345	1.355	
D_2	33.02		Reference	1.300		Reference
E	7.62	8.62		0.300	0.339	
E_1	6.86	7.37		0.270	0.290	
e_1	2.54		Reference	0.100		Reference
e_A	7.62		Reference	0.300		Reference
e_B	7.62	10.16		0.300	0.400	
L	3.18	3.43		0.125	0.135	
N	28		300 MIL	28		300 MIL
S	0.051	0.76		0.020	0.030	
S_1	0.23			0.009		

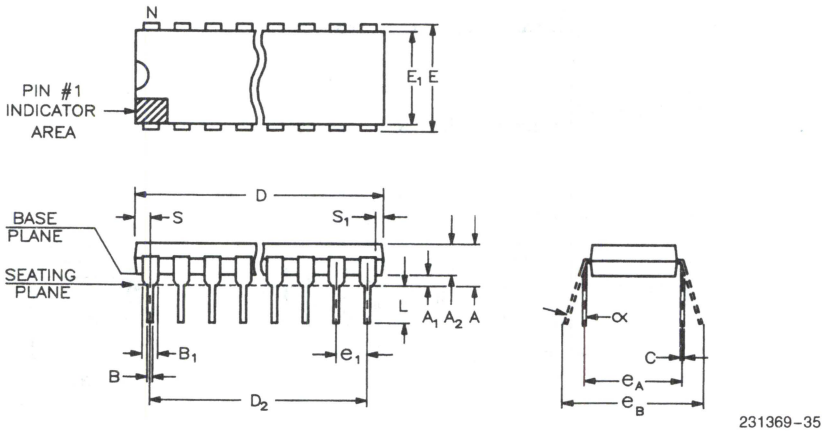
28 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.68	4.06		0.145	0.160	
B	0.36	0.56		0.014	0.022	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	36.70	37.34		1.445	1.470	
D_2	33.02		Reference	1.300		Reference
E		15.75			0.620	
E_1	13.59	14.0		0.535	0.551	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	28		600 MIL	28		600 MIL
S	1.65	2.16		0.065	0.085	
S_1	0.86			0.034		

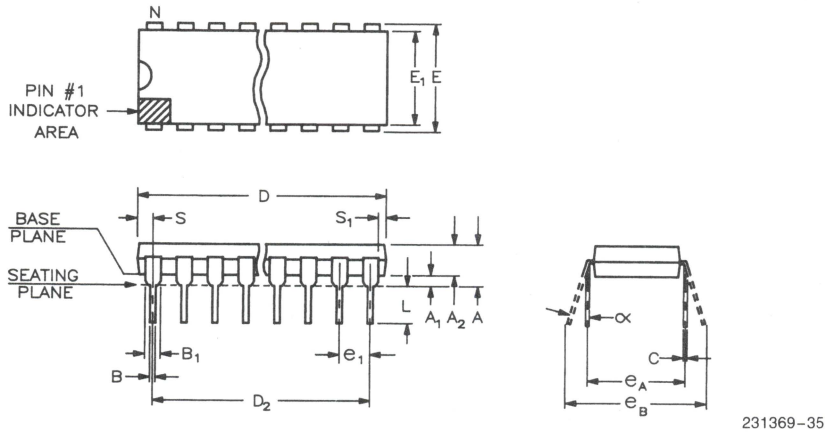
32 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.83			0.190	
A_1	0.38			0.015		
A_2	3.81		Typical	0.150		Typical
B	0.41	0.51		0.016	0.020	
B_1	1.14	1.40		0.045	0.055	
C	0.20	0.30		0.008	0.012	
D	41.78	42.04		1.645	1.655	
D_2	38.10		Reference	1.500		Reference
E	15.24	15.88		0.600	0.625	
E_1	13.46	13.97		0.530	0.550	
e_1	2.54		Reference	0.100		Reference
e_A	15.24		Reference	0.600		Reference
e_B	15.24	17.78		0.600	0.700	
L	3.18	3.43		0.125	0.135	
N	32		600 MIL	32		600 MIL
S	1.78	2.03		0.070	0.080	
S_1	1.14			0.045		

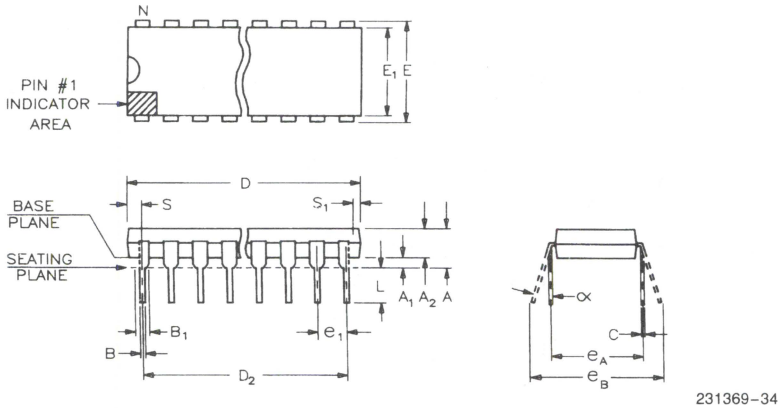
40 LEAD PLASTIC DUAL IN-LINE PACKAGE



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.94	4.19		0.155	0.165	
B	0.41	0.51		0.016	0.020	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30		0.009	0.012	
D	51.94	52.58		2.045	2.070	
D_2	48.26		Reference	1.900		Reference
E		15.75			0.620	
E_1	13.59	13.84		0.535	0.545	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	40			40		
S	1.65	2.16		0.065	0.085	
S_1	0.99			0.039		

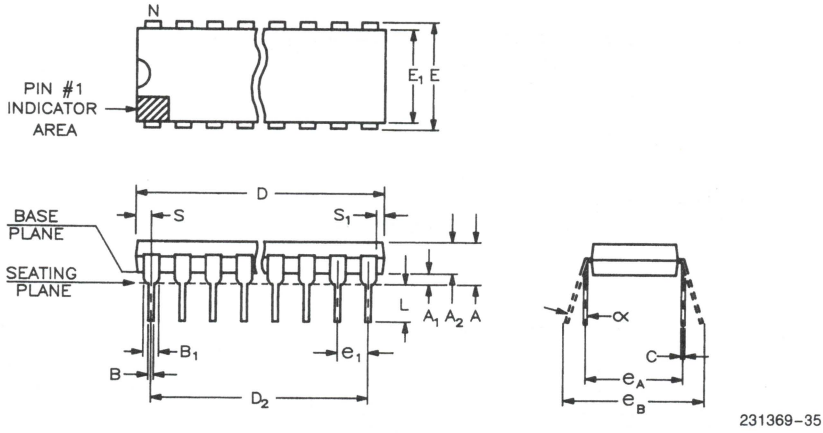
40 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: ½ LEAD



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
a	0°	10°		0°	10°	
A	4.55			0.179		
A_1	0.38			0.015		
A_2	3.75	3.95	Nom 3.85	0.147	0.155	
B	0.35	0.51		0.014	0.020	
B_1	1.4	1.6		0.055	0.063	
C	0.25	0.45	Nom 0.35	0.009	0.018	
D		52.3			2.06	
D_2						
E	13.5	13.9	Nom 13.7	0.531	0.547	
E_1						
e_1	2.29	2.79	Nom 2.54	0.090	0.110	
e_A	14.74	15.74	Nom 15.24	0.580	0.619	
e_B						
L	3.0	3.6	Nom 3.3	0.118	0.141	
N	40		½ Lead	40		½ Lead
S	1.65	2.16		0.065	0.080	
S_1						

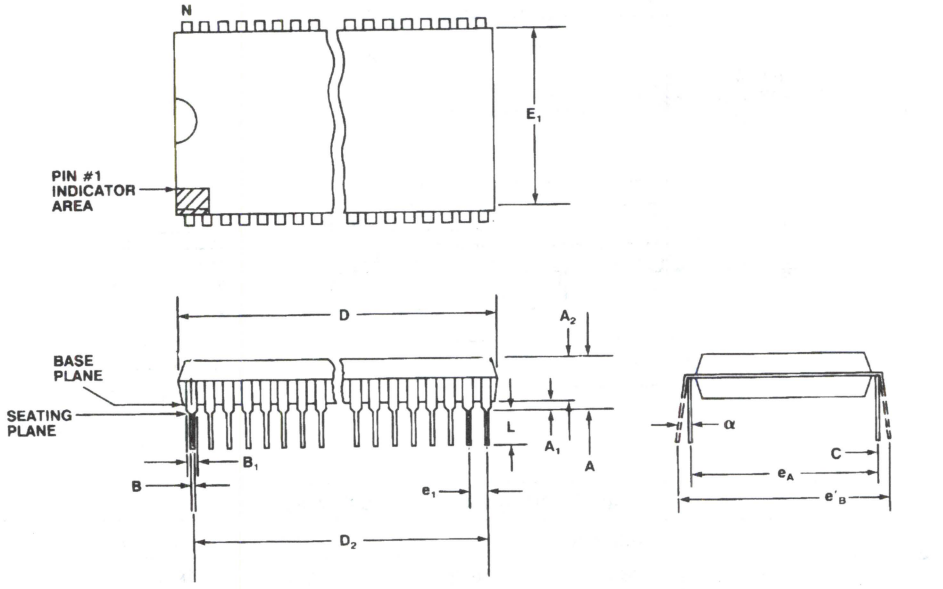
48 LEAD PLASTIC DUAL IN-LINE PACKAGE



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.94	4.32		0.155	0.170	
B	0.41	0.51		0.016	0.020	
B_1	1.27		Typical	0.050		Typical
C	0.23	0.30		0.009	0.012	
D	61.60	61.98		2.425	2.440	
D_2	58.42		Reference	2.300		Reference
E		15.75			0.620	
E_1	13.84	14.10		0.545	0.555	
e_1	2.29	2.79		0.090	0.110	
e_A	14.99		Reference	0.590		Reference
e_B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	48			48		
S	1.65	2.16		0.065	0.085	
S_1	0.99	1.40		0.039	0.055	

64 LEAD PLASTIC DUAL IN-LINE PACKAGE (SHRINK)



231369-36

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		5.65			0.22	
A_1	0.51			0.020		
A_2	4.15	4.35		0.163	0.171	
B	0.35	0.55		0.014	0.022	
B_1	1.0		Typical	0.040		Typical
C	0.20	0.30		0.008	0.012	
D	57.8	58.2		2.28	2.29	
D_2	55.12		Reference	2.170		Reference
E						
E_1	16.8	17.2		0.661	0.677	
e_1	1.60	1.96		0.063	0.077	
e_A	19.05			0.745 BSC		
e_B	19.5	21.0		0.767	0.826	
L	3.0	3.6		0.118	0.142	
N	64			64		

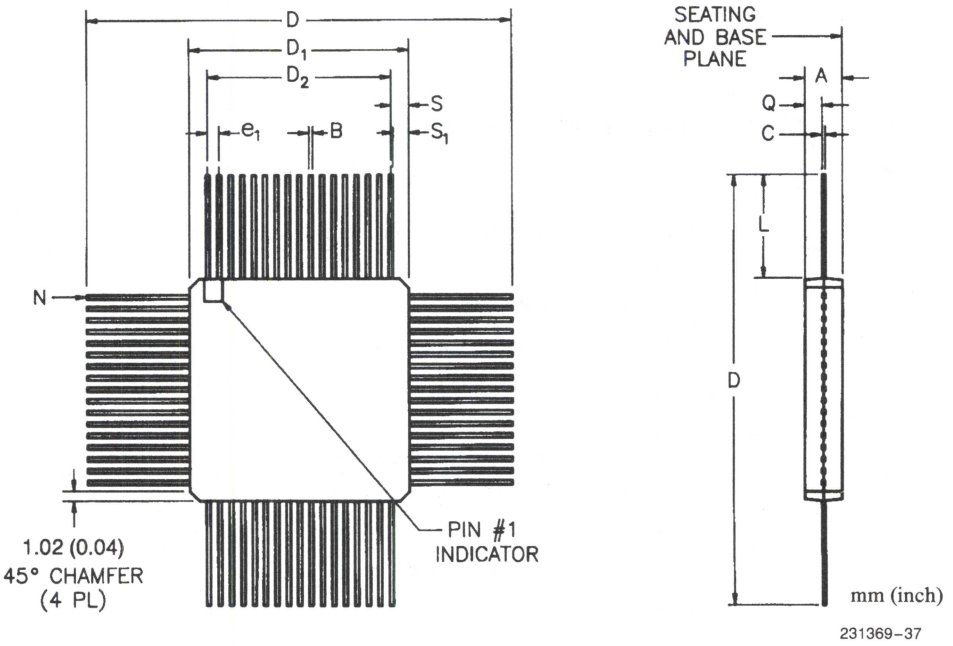
PLASTIC FLATPACK PACKAGE

Symbol List for Plastic Flatpack Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_1	Largest overall package dimension of length excluding leads
D_2	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between centerlines of terminal leads
L	Lead dimension free lead length
N	The total number of potentially useable lead positions
Q	Lead plane to top of body plane distance
S	Distance from true position centerline of end lead position to the extremity of the body
S_1	Linear spacing of true maximum lead position from lead edge to package edge

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.

68 LEAD PLASTIC FLATPACK PACKAGE



Family: Plastic Flatpack Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.19	4.34		0.165	0.171	
B	0.46	0.56		0.018	0.022	Typical
C	0.18	0.25		0.007	0.010	Typical
D	44.45	45.21		1.750	1.780	
D_1	24.08	24.26		0.948	0.955	
D_2	20.22	20.42		0.796	0.804	
e_1	1.22	1.32	Typical	0.048	0.052	Typical
L	10.16	10.80		0.400	0.425	
N	68			68		
Q	2.01	2.06		0.079	0.081	
S	1.73	2.08		0.068	0.082	
S_1	1.47			0.058		

PLASTIC LEADED CHIP CARRIER PACKAGE

Symbol List for Plastic Leaded Chip Carrier Family

Letter or Symbol	Description of Dimensions
A	Overall Height: Distance from seating plane to highest point of body
A_1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Overall package dimension
D_1/E_1	Plastic body dimension
D_2/E_2	Footprint
LT	Lead thickness
N	Total number of leads
N_d	Total number of leads on short side
N_e	Total number of leads on long side
TCP	Tweezing coplanarity

NOTES RECTANGLE PACKAGE:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **—H—** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **A—B** and **—D—** to be determined where center leads exit plastic body at datum plane **—H—**.
4. To be determined at seating plane **—C—**.
5. Dimensions D_1 and E_1 do not include mold protrusion.
6. Pin 1 identifier is located within the defined zone.
7. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
8. N_d denotes the number of leads on the two short sides of the package, one of which contains pin #1. N_e denotes the number of leads on the two long sides of the package.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **A—B** or **—D—**.

Packaging Family Attributes	
Category	Plastic Leaded Chip Carrier
Acronym	PLCC
Lead Configuration	Quad
Lead Counts	28, 32, 44, 52, 68, 84
Lead Finish	SolderPlate
Lead Pitch	0.050″
Board Assembly Type	Socket and Surface Mount

NOTES:

1. Copper Alloy Leads.
2. Novalac Body.
3. Bake and dessicant packaging required.

Family: Plastic Leaded Chip Carrier-Rectangular (mm)						
Symbol	28 Lead			32 Lead		
	Min	Max	Notes	Min	Max	Notes
A	3.20	3.56		3.20	3.56	
A_1	1.93	2.29		1.93	2.29	
D	9.78	10.0		12.3	12.6	
D_1	8.81	8.97		11.4	11.5	
D_2	7.37	8.38		9.91	10.9	
E	14.9	15.1		14.9	15.1	
E_1	13.9	14.0		13.9	14.0	
E_2	12.4	13.5		12.4	13.5	
N	28			32		
N_d	5			7		
N_e	9			9		
CP	0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10	
LT	0.23	0.38		0.23	0.38	

Family: Plastic Leaded Chip Carrier-Rectangular (inch)						
Symbol	28 Lead			32 Lead		
	Min	Max	Notes	Min	Max	Notes
A	0.126	0.140		0.126	0.140	
A_1	0.076	0.090		0.076	0.090	
D	0.385	0.395		0.485	0.495	
D_1	0.347	0.353		0.447	0.453	
D_2	0.290	0.330		0.390	0.430	
E	0.585	0.595		0.585	0.595	
E_1	0.547	0.553		0.547	0.553	
E_2	0.490	0.530		0.490	0.530	
N	28			32		
N_d	5			7		
N_e	9			9		
CP	0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004	
LT	0.009	0.015		0.009	0.015	

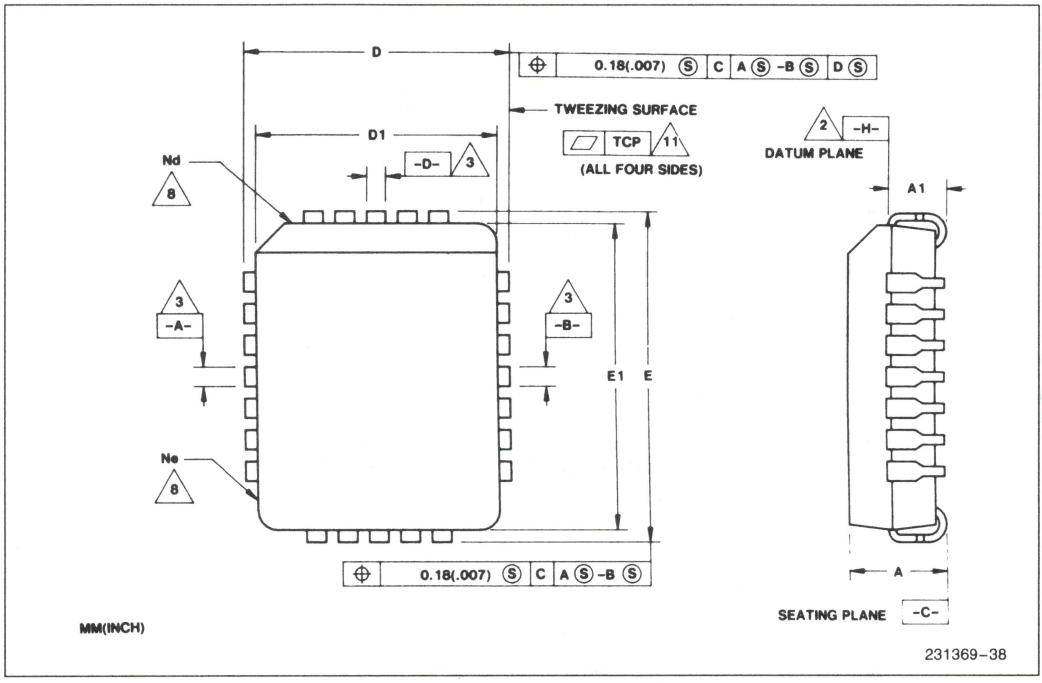


Figure 1. Principal Dimensions and Datums

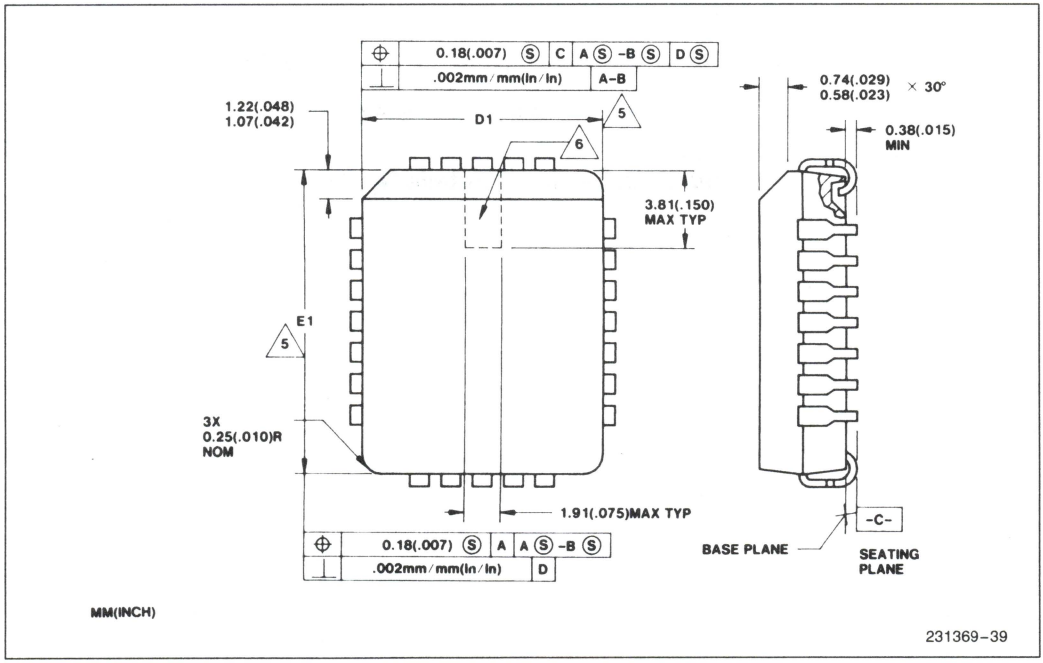


Figure 2. Molded Details

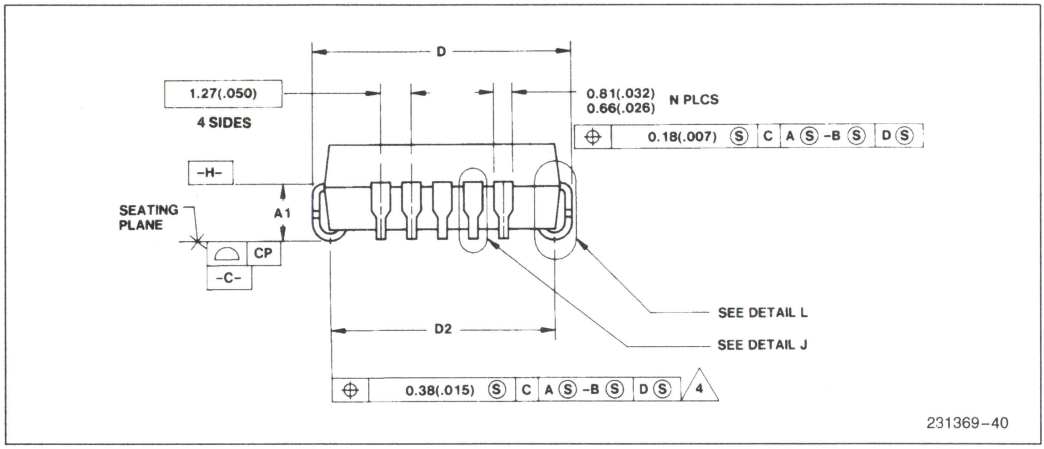


Figure 3A. Terminal Details N_D Side

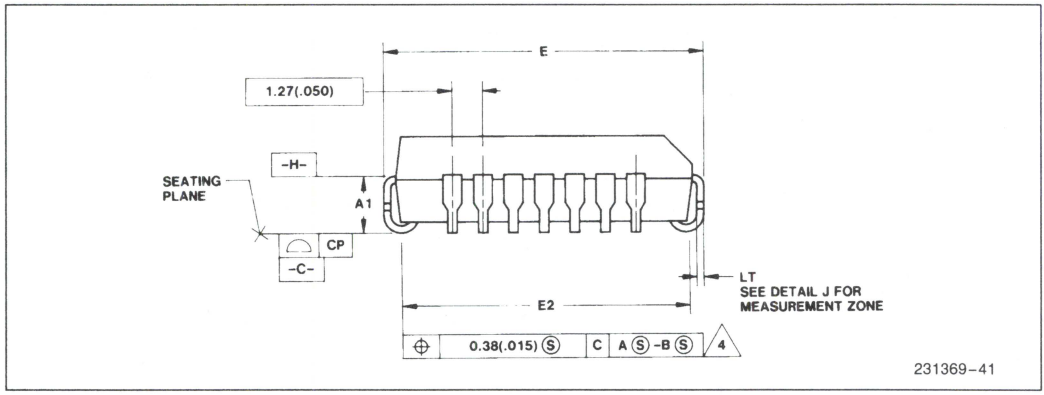


Figure 3B. Terminal Details N_E Side

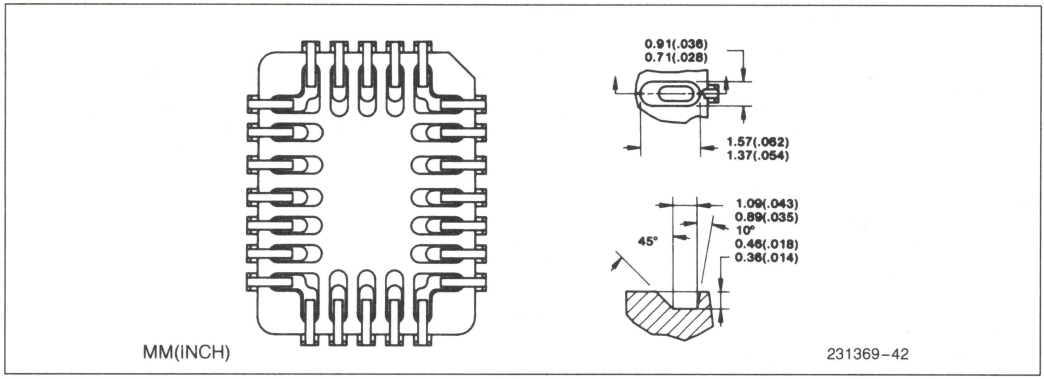


Figure 4. Standard Package Bottom View

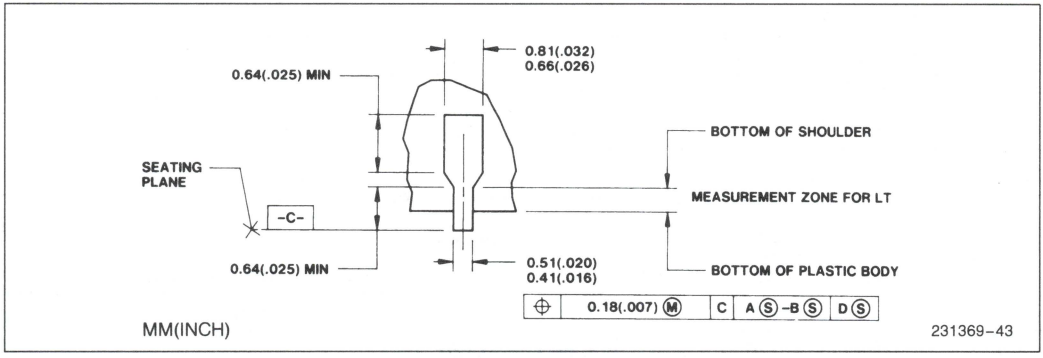


Figure 5. Detail J. Terminal Details

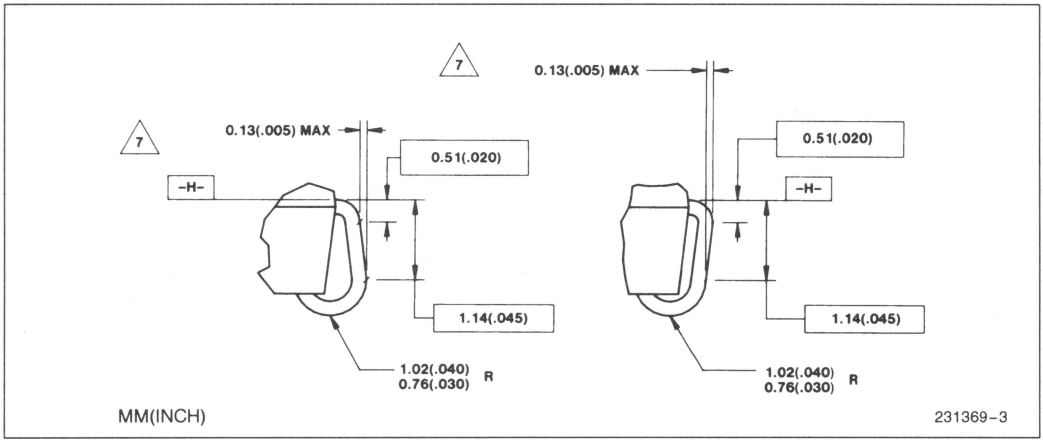


Figure 6. Detail L. Terminal Details

Family: Plastic Leaded Chip Carrier-Square (mm)									
Symbol	20 Lead			28 Lead			44 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		4.19	4.57		4.19	4.57	
A_1	2.29	3.05		2.29	3.05		2.29	3.05	
D	9.78	10.0		12.3	12.6		17.4	17.7	
D_1	8.89	9.04		11.4	11.6		16.5	16.7	
D_2	7.37	8.38		9.91	10.9		15.0	16.0	
E	9.78	10.0		12.3	12.6		17.4	17.7	
E_1	8.89	9.04		11.4	11.6		16.5	16.7	
E_2	7.37	8.38		9.91	10.9		15.0	16.0	
N	20			28			44		
CP	0.00	0.10		0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10		0.00	0.10	
LT	0.23	0.38		0.23	0.38		0.23	0.38	

Family: Plastic Leaded Chip Carrier-Square (inch)									
Symbol	20 Lead			28 Lead			44 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	0.165	0.180		0.165	0.180		0.165	0.180	
A_1	0.090	0.120		0.090	0.120		0.090	0.120	
D	0.385	0.395		0.485	0.495		0.685	0.695	
D_1	0.350	0.356		0.450	0.456		0.650	0.656	
D_2	0.290	0.330		0.390	0.430		0.590	0.630	
E	0.385	0.395		0.485	0.495		0.685	0.695	
E_1	0.350	0.356		0.450	0.456		0.650	0.656	
E_2	0.290	0.330		0.390	0.430		0.590	0.630	
N	20			28			44		
CP	0.000	0.004		0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004		0.000	0.004	
LT	0.009	0.015		0.009	0.015		0.009	0.015	

Family: Plastic Leaded Chip Carrier-Square (mm)									
Symbol	52 Lead			68 Lead			84 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		4.19	4.83		4.19	4.83	
A_1	2.29	3.05		2.29	3.05		2.29	3.05	
D	19.9	20.2		25.0	25.3		30.1	30.4	
D_1	19.1	19.2		24.1	24.3		29.2	29.4	
D_2	17.5	18.5		22.6	23.6		27.7	28.7	
E	19.9	20.2		25.0	25.3		30.1	30.4	
E_1	19.1	19.2		24.1	24.3		29.2	29.4	
E_2	17.5	18.5		22.6	23.6		27.7	28.7	
N	52			68			84		
CP	0.00	0.10		0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10		0.00	0.10	
LT	0.23	0.38		0.20	0.36		0.20	0.36	

Family: Plastic Leaded Chip Carrier-Square (inch)									
Symbol	52 Lead			68 Lead			84 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	0.165	0.180		0.165	0.190		0.165	0.190	
A_1	0.090	0.120		0.090	0.120		0.090	0.120	
D	0.785	0.795		0.985	0.995		1.185	1.195	
D_1	0.750	0.756		0.950	0.958		1.150	1.158	
D_2	0.690	0.730		0.890	0.930		1.090	1.130	
E	0.785	0.795		0.985	0.995		1.185	1.195	
E_1	0.750	0.756		0.950	0.958		1.150	1.158	
E_2	0.690	0.730		0.890	0.930		1.090	1.130	
N	52			68			84		
CP	0.000	0.004		0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004		0.000	0.004	
LT	0.009	0.015		0.008	0.014		0.008	0.014	

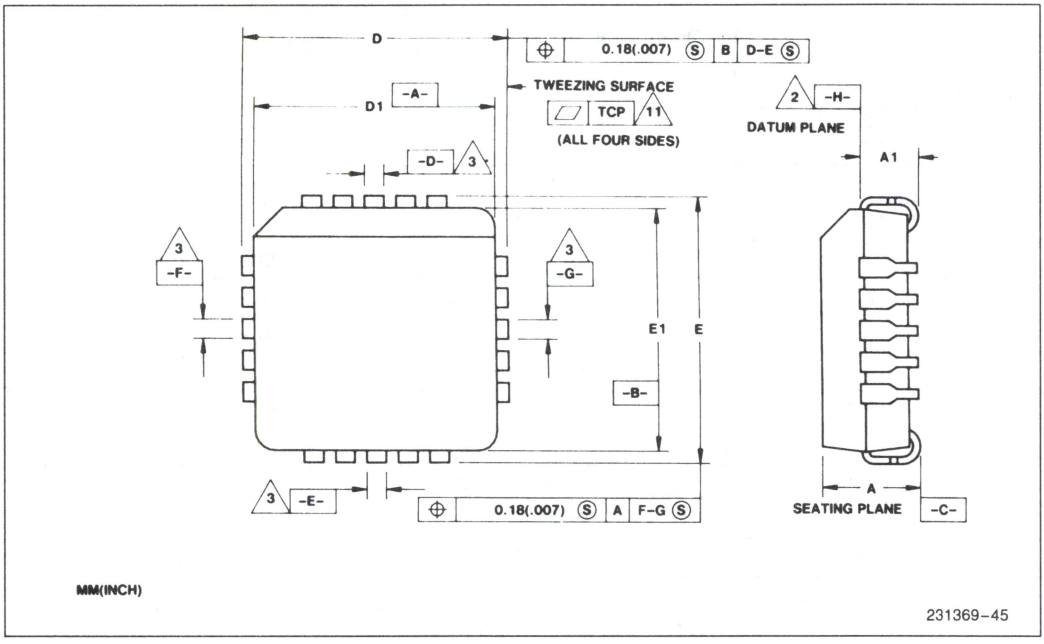


Figure 1. Principal Dimensions and Datums

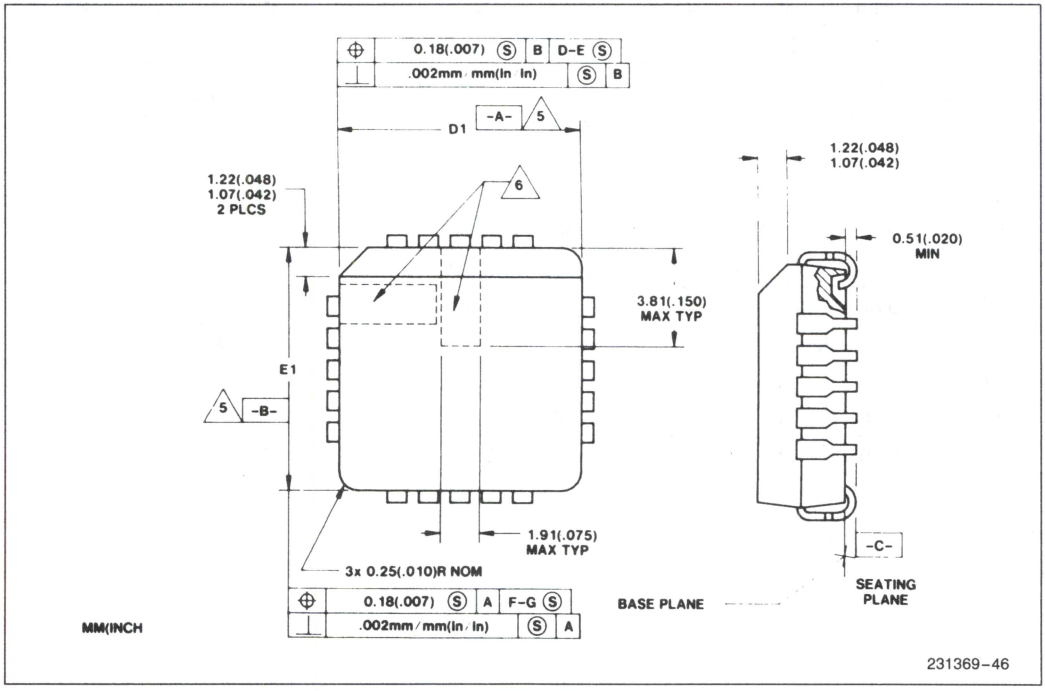


Figure 2. Molded Details

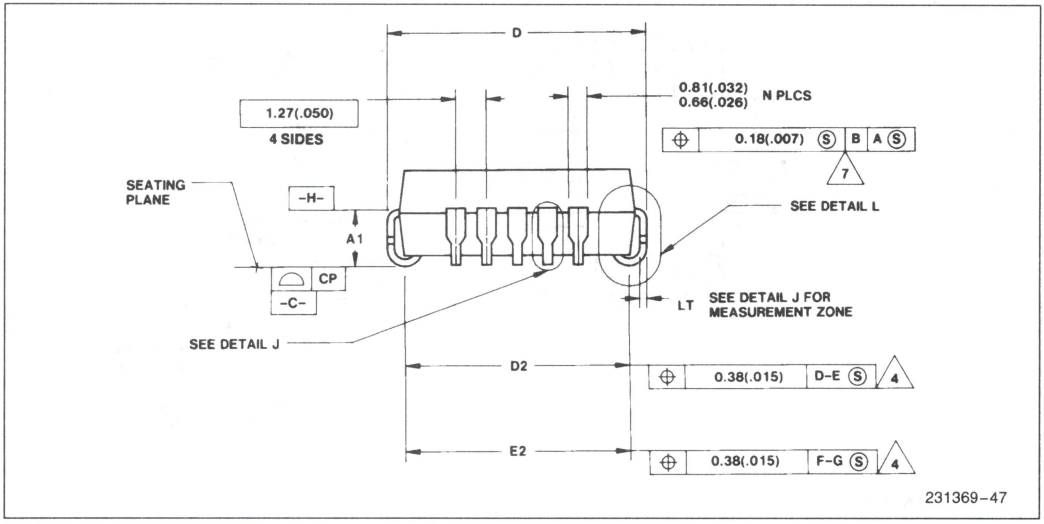


Figure 3. Terminal Details

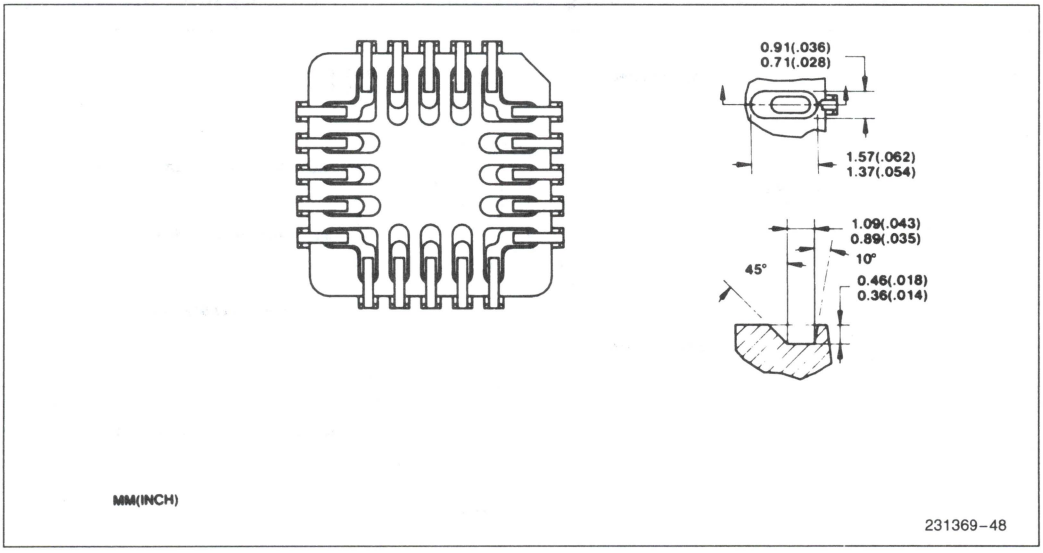


Figure 4A. Standard Package Bottom View (Tooling Option I.)

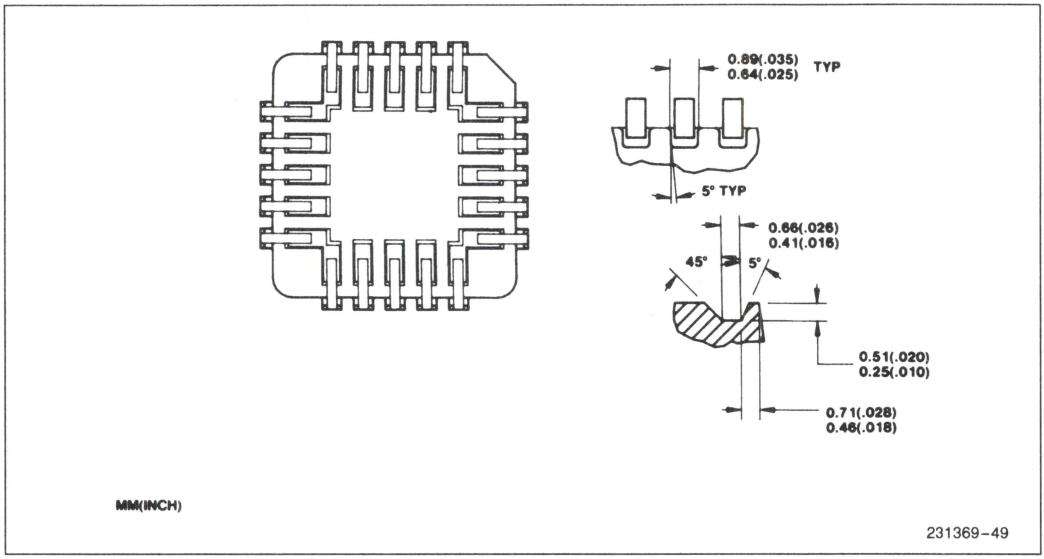


Figure 4B. Standard Package Bottom View (Tooling Option II.)

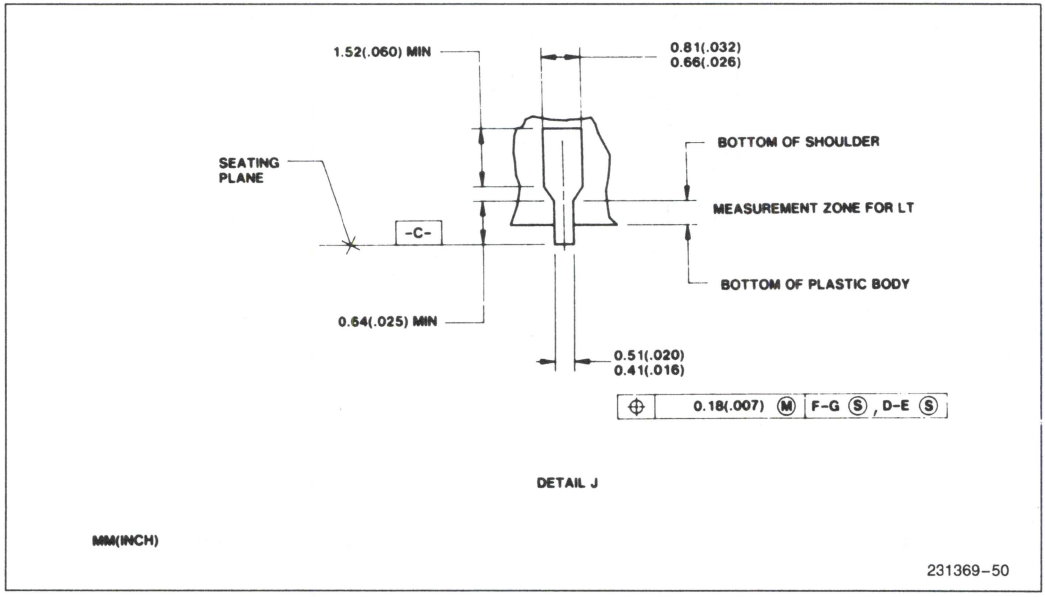


Figure 5. Detail J. Terminal Detail

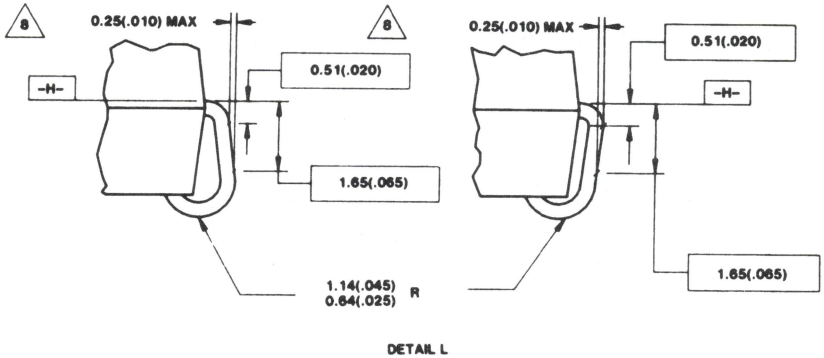


Figure 6. Detail L. Terminal Details

NOTES SQUARE PACKAGE:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **—H—** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **D—E** and **F—G** to be determined where center leads exit plastic body at datum plane **—H—**.
4. To be determined at seating plane **—C—**.
5. Dimensions D_1 and E_1 do not include mold protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum **—A—** and **—B—** to be determined at plane **—H—**.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **D—E** or **F—G**.

PLASTIC QUAD FLATPACK PACKAGE

Symbol List for Plastic Quad Flatpack Family

Symbol	Description
N	Leadcount
A	Package Height
A1	Standoff
D, E	Terminal Dimension
D1, E1	Package Body
D2, E2	Bumper Distance
D3, E3	Foot Print
D4, E4	Foot Radius Location
L1	Foot Length

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A-B and -D- to be determined where center leads exit plastic body at datum plane -H-.
4. Controlling Dimension, Inch.
5. Dimensions D1, D2, E1 and E2 are measured at the mold parting line. D1 and E1 do not include an allowable mold protrusion of 0.25 mm (0.010 in) per side. D2 and E2 do not include a total allowable mold protrusion of 0.25 mm (0.010 in) at maximum package size.
6. Pin 1 identifier is located within one of the two zones indicated.
7. Measured at datum plane -H-.
8. Measured at seating plane datum -C-.

Packaging Family Attributes	
Category	Plastic Quad Flatpack
Acronym	PQFP
Lead Configuration	Gull-Wing
Lead Counts	84, 100, 132, 164, 196
Lead Finish	SolderPlate
Lead Pitch	0.025″
Board Assembly Type	Surface or Socket Mount

Plastic Quad Flatpack (PQFP) 0.025 Inch (0.635mm) Pitch											
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Leadcount	84		100		132		164		196	
A	Package Height	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
A1	Standoff	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
D, E	Terminal Dimension	0.770	0.790	0.870	0.890	1.070	1.090	1.270	1.290	1.470	1.490
D1, E1	Package Body	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
											INCH

Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Leadcount	84		100		132		164		196	
A	Package Height	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57
A1	Standoff	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
D, E	Terminal Dimension	19.56	20.07	22.01	22.61	27.18	27.69	32.26	32.77	37.34	37.85
D1, E1	Package Body	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	18.36	18.71	20.90	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
											mm

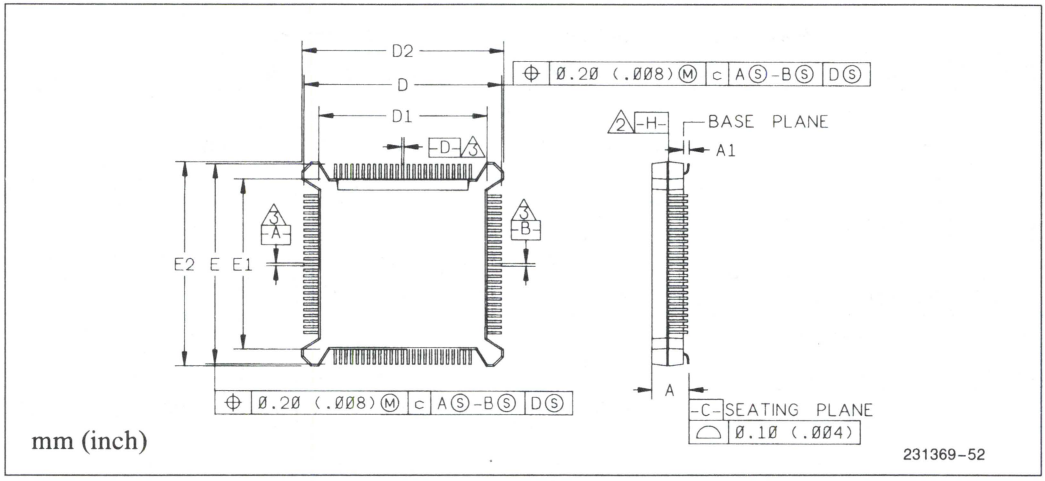


Figure 1. Principal Dimensions and Datums

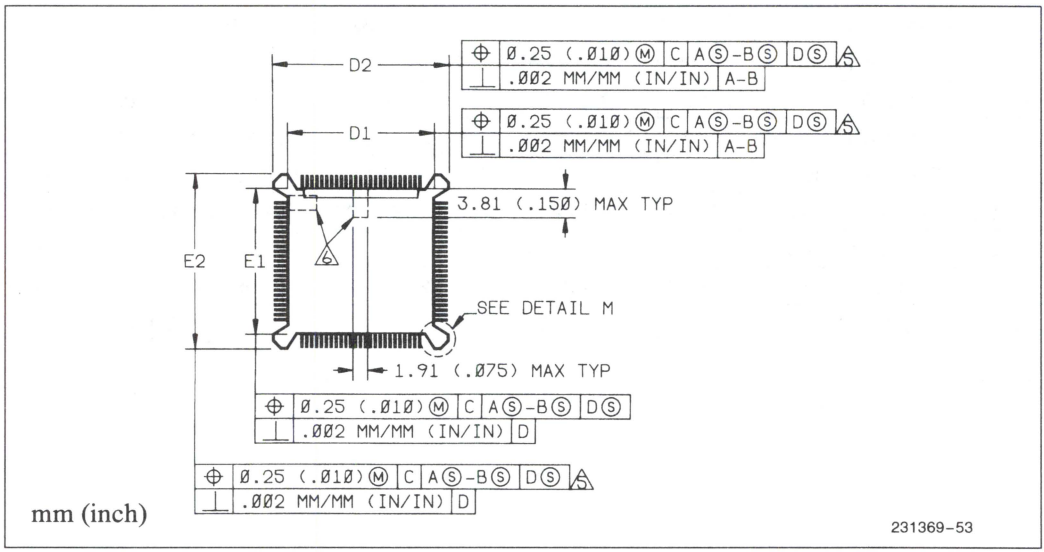
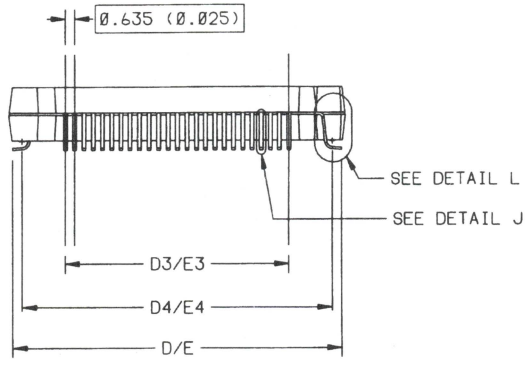


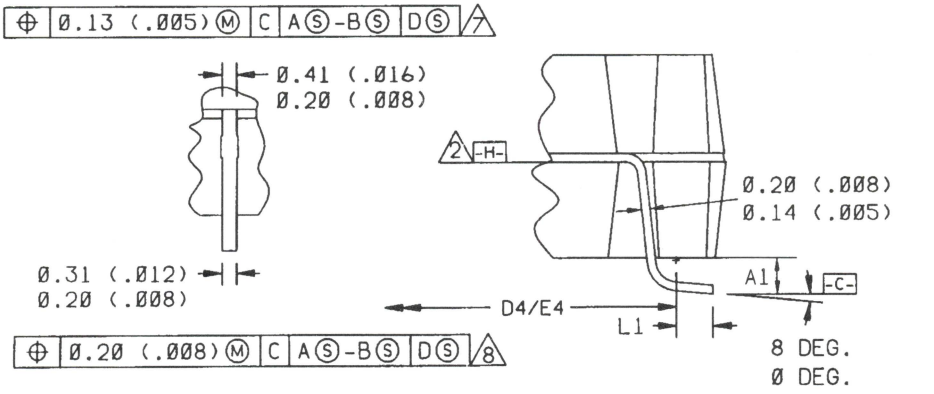
Figure 2. Molded Details



mm (inch)

231369-54

Figure 3. Terminal Details

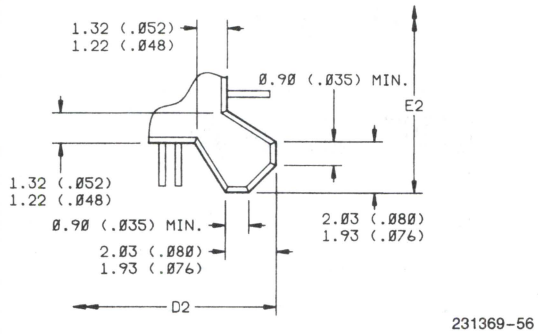


mm (inch)

231369-55

Detail J **Detail L**

Figure 4. Typical Lead



mm (inch)

Figure 5. Detail M

QUAD FLATPACK PACKAGE

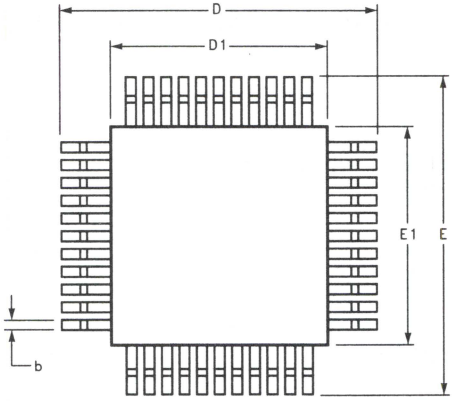
Symbol List for Quad Flatpack Family

Letter or Symbol	Description of Dimensions
N	Lead Count
A	Overall Height
A_1	Stand Off
AAA	Lead True Position
B	Lead Width
C	Lead Thickness
D	Terminal Dimension
D_1	Body Package
E	Terminal Dimension
E_1	Body Package
e_1	Lead Pitch
L_1	Foot Length
T	Lead Angle
Y	Coplanarity

NOTE:
4. Not all packages are available with all products. Contact local FSE for further package information.

Packaging Family Attributes	
Category	Quad Flatpack
Acronym	QFP, SQFP, TQFP
Lead Configuration	Quad
Lead Counts	QFP 44, 48, 64, 80, 100, 128, 160 - SQFP 80, 100, 208 - TQFP 144, 176
Lead Finish	SolderPlate
Lead Pitch	0.5, 0.65, 0.8 mm
Board Assembly Type	Socket and Surface Mount

NOTE:
1. QFP - Alloy 42/copper on some lead frames. SQFP/TQFP copper lead frames only.
2. Novalac body.
3. Not all packages are available with all products. Contact local FSE for further package information.



NOTE:
All dimensions in millimeters

Figure 1. Principal Dimensions and Data for QFP (square)/TQFP/SQFP Packages

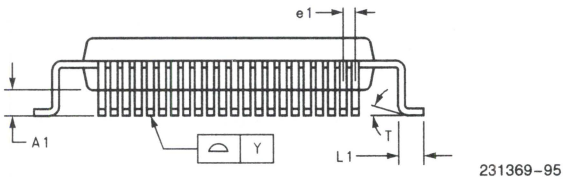


Figure 2. Terminal Details

Quad Flatpack (Square Packages)														
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Max**	**Min**	**Max**
N	Lead Count		44			48			64		128		160	
A	Overall Height			2.35			2.55			2.55	3.25	3.75	3.25	3.75
A_1	Stand Off	0.00			0.05		0.25	0.00			0	0.30	0	0.30
b	Lead Width	0.20	0.30	0.40	0.25	0.30	0.40	0.20	0.30	0.40	0.25	0.45	0.20	0.40
c	Lead Thickness	0.10	0.15	0.20	0.11	0.15	0.20	0.10	0.15	0.20	0.150	0.188	0.150	0.188
D	Terminal Dimension	12.0	12.4	12.8	15.1	15.3	15.5	14.9	15.3	15.7	31.6	32.4	31.6	32.4
D_1	Package Body		10.0		11.9	12.0	12.1		12.0		27.9	28.1	27.9	28.1
E	Terminal Dimension	12.0	12.4	12.8	15.1	15.3	15.5	14.9	15.3	15.7	31.6	32.4	31.6	32.4
E_1	Package Body		10.0		11.9	12.0	12.1		12.0		27.9	28.1	27.9	28.1
e_1	Lead Pitch	0.65	0.80	0.95	0.70	0.80	0.90	0.53	0.65	0.77	0.70	0.90	0.55	0.75
L_1	Foot Length	0.38	0.58	0.78	0.65	0.85	1.05	0.65	0.85	1.05	0.60	1.0	0.60	1.0
T	Lead Angle	0.0°		10.0°	0.0°		7.0°	0.0°		10.0°	0°	10°	0°	10°
Y	Coplanarity			0.10			0.10			0.10	0.1		0.1	

NOTE:
1. Dimensions are in millimeters.

Shrink Quad Flatpack									
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Max**
N	Lead Count		80			100		208	
A	Overall Height			1.66			1.66	3.25	3.75
A_1	Stand Off	0.00			0.00			0	0.30
b	Lead Width	0.14	0.20	0.26	0.14	0.20	0.26	0.14	0.26
c	Lead Thickness	0.117	0.127	0.177	0.117	0.127	0.177	0.150	0.188
D	Terminal Dimension	13.70	14.00	14.30	15.70	16.0	16.30	30.2	31.0
D_1	Package Body		12.0			14.0		27.9	28.1
E	Terminal Dimension	13.70	14.0	14.30	15.70	16.00	16.30	30.2	31.0
E_1	Package Body		12.0			14.0		27.9	28.1
e_1	Lead Pitch	0.40	0.50	0.60	0.40	0.50	0.60	0.40	0.60
L_1	Foot Length	0.35	0.50	0.70	0.30	0.50	0.70	0.30	0.70
T	Lead Angle	0.0°		10.0°	0.0°		10.0°	0.0°	10.0°
Y	Coplanarity			0.10			0.10	0.1	

Thin Quad Flatpack					
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**
N	Lead Count	144		176	
A	Overall Height	1.3	1.7	1.3	1.7
A_1	Stand Off	0	0.20	0	0.20
b	Lead Width	0.16	0.28	0.16	0.28
c	Lead Thickness	0.122	0.160	0.122	0.160
D	Terminal Dimension	21.6	22.4	25.6	26.4
D_1	Package Body	19.9	20.1	23.9	24.1
E	Terminal Dimension	21.6	22.4	25.6	26.4
E_1	Package Body	19.9	20.1	23.9	24.1
e_1	Lead Pitch	0.40	0.60	0.40	0.60
L_1	Foot Length	0.40	0.80	0.40	0.80
T	Lead Angle	0.0°	10.0°	0.0°	10.0°
Y	Coplanarity	0.1		0.1	

NOTE:
1. Dimensions are in millimeters.

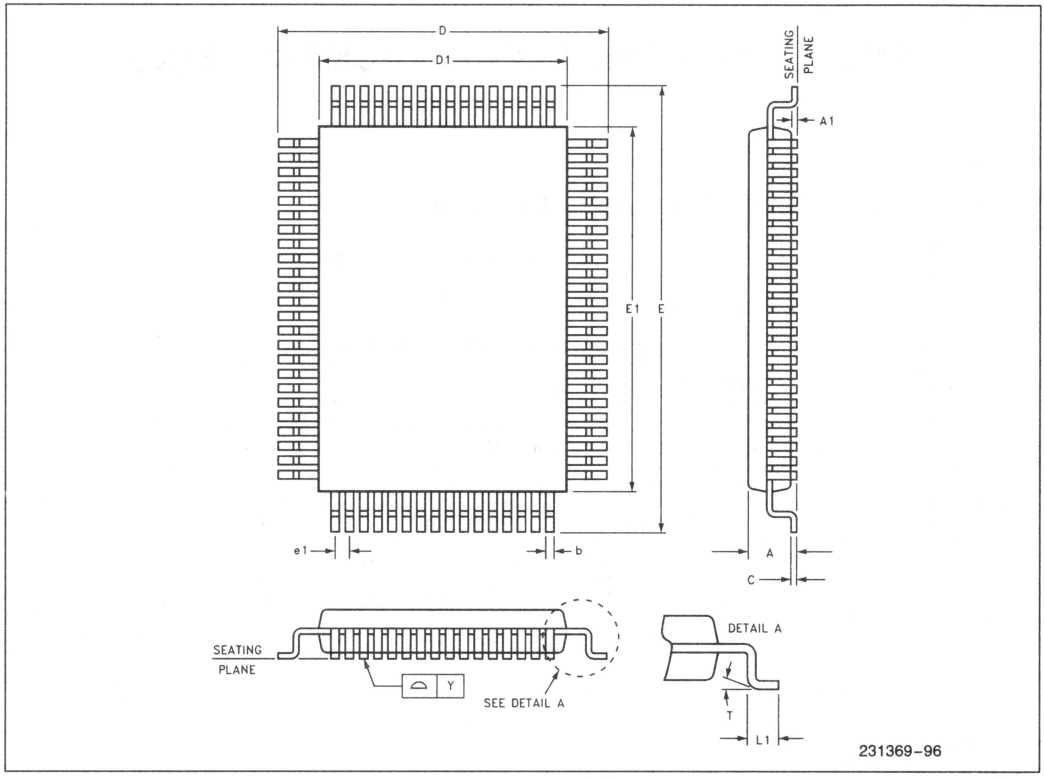


Figure 3. Principle Dimensions and Data for QFP (Rectangular) Packages

Quad Flatpack (Rectangular Packages)							
Symbol	**Description**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
N	Lead Count		80			100	
A	Overall Height			3.15			3.15
A_1	Stand Off	0.00			0.00		
b	Lead Width	0.25	0.35	0.45	0.20	0.30	0.40
c	Lead Thickness	0.10	0.15	0.20	0.10	0.15	0.20
D	Terminal Dimension	17.5	17.9	18.3	17.5	17.9	18.3
D_1	Package Body		14.0			14.0	
E	Terminal Dimension	23.5	23.9	24.3	23.5	23.9	24.3
E_1	Package Body		20.0			20.0	
e_1	Lead Pitch	0.65	0.80	0.95	0.53	0.65	0.77
L_1	Foot Length	0.60	0.80	1.00	0.60	0.80	1.00
T	Lead Angle	0.0°		10.0°	0.0°		10.0°
Y	Coplanarity			0.10			0.10

SMALL OUT-LINE J-LEAD PACKAGE (SOJ)

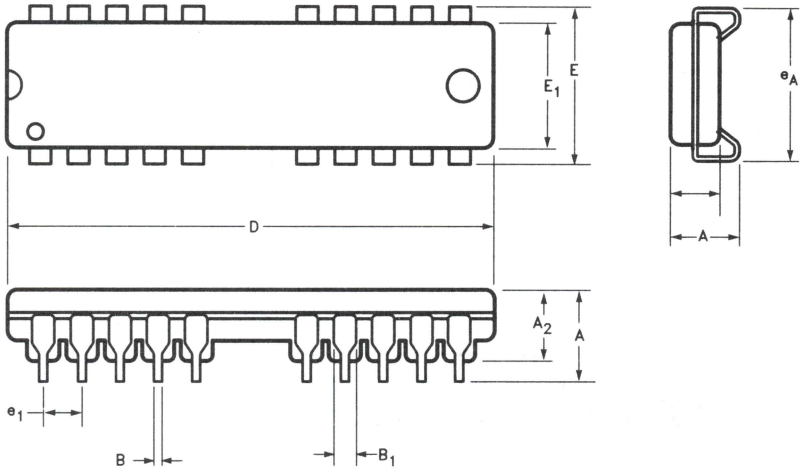
Symbol List for Small Out-Line J-Lead Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_2	Distance from Base Plane to Highest Point of Body (Lid)
B	Width of Terminal Leads
B_1	Width of Terminal Lead Shoulder Which Locate Seating Plane (Standoff Geometry Optional)
D	Largest Overall Package Dimension of Length
E	Largest Overall Package Width Dimension Outside of Leads
E_1	Body Width Dimension Not Including Leads
e_1	Linear Spacing between Center Line of Body Terminal Leads (Standoffs)
e_A	Linear Spacing of True Minimum Lead Position Center Line to Center Line
N	Total Number of Leads

Packaging Family Attributes	
Category	Small Outline J-Lead
Acronym	SOJ
Lead Configuration	Dual-In-Line
Lead Counts	20, 24
Lead Finish	SolderPlate
Lead Pitch	0.050″
Board Assembly Type	Surface Mount

NOTES:
1. Alloy 42 Leads.
2. Novalac Body.

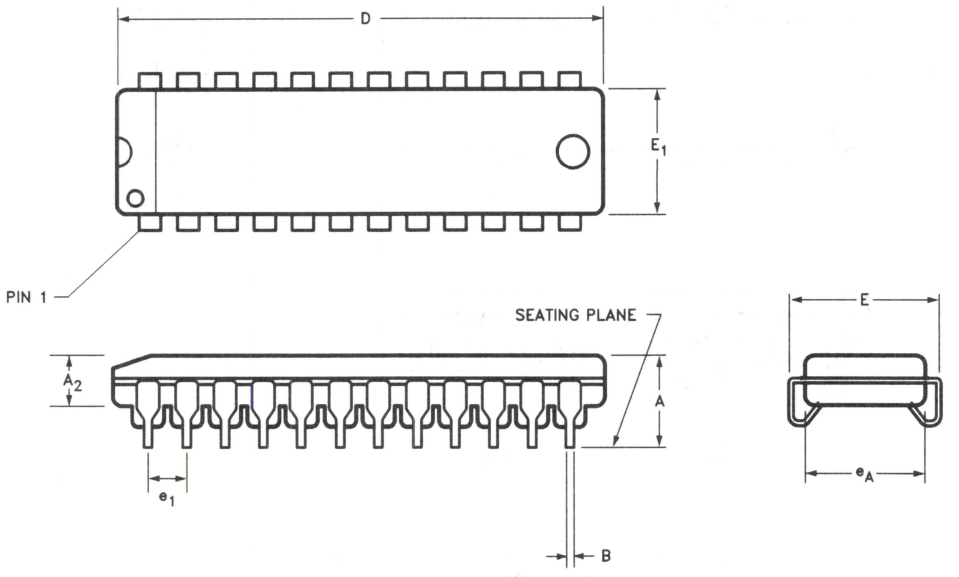
20 LEAD SMALL OUT-LINE PACKAGE (SOJ) VARIATION: J-LEAD



231369-61

Family: Small Out-Line J-Lead Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.04	3.61		0.120	0.142	
A_2	2.36	3.00		0.093	0.118	
B	0.38	0.51		0.015	0.020	
B_1	0.58	0.84		0.023	0.033	
D	17.02	17.27		0.67	0.680	
E	8.31	8.64		0.327	0.340	
E_1	7.49	7.75		0.295	0.305	
e_1	1.27		Typical	0.050		Typical
e_A	6.60	6.99		0.260	0.275	
e_B	7.62	10.16		0.300	0.400	
N	20			20		

24 LEAD SMALL OUT-LINE PACKAGE (SOJ) VARIATION: J-LEAD



231369-62

Family: Small Out-Line J-Lead Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α						
A	3.35	3.61		0.132	0.142	
A_1						
A_2	2.74	3.00		0.108	0.118	
A_3						
B	0.38	0.51		0.015	0.020	
D	15.75	16.18		0.620	0.637	
D_2						
E	8.38	8.64		0.330	0.340	
E_1	7.49	7.75		0.295	0.305	
e_1	1.27		Typical	0.050		Typical
e_A	6.60	6.99		0.260	0.275	
e_B						
L						
N	24			24		

SMALL OUT-LINE PACKAGE (SOP)

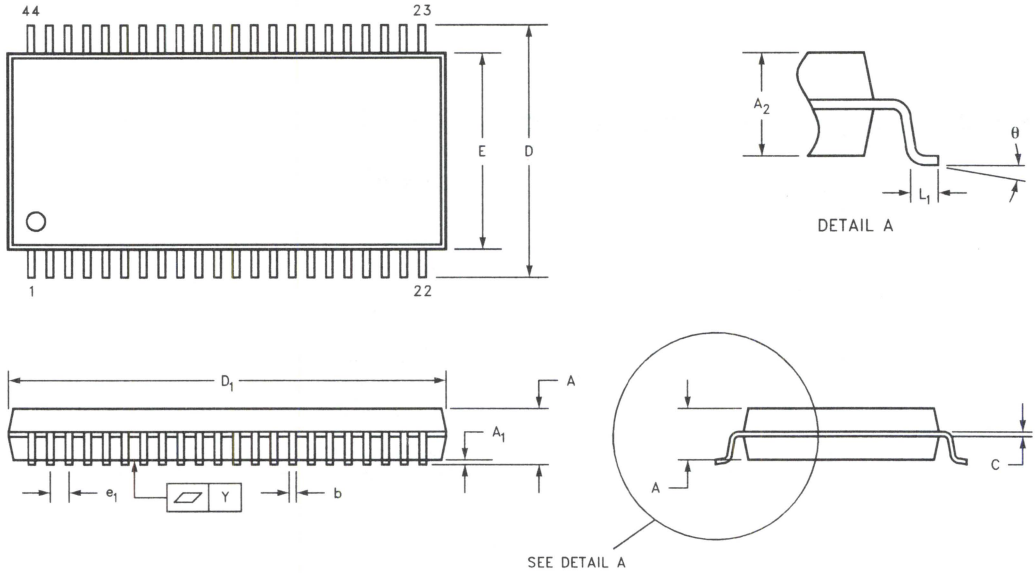
Symbol List for Small Out-Line Package Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Standoff
A_2	Package Body Thickness
b	Lead Width
c	Lead Thickness
D_1	Plastic Body Length
E	Package Body Width
e_1	Lead Pitch
D	Terminal Dimension
L_1	Lead Foot Length
N	Total Number of Leads
Y	Coplanarity
θ	Lead Tip Angle

Packaging Family Attributes	
Category	Small Out-Line Package
Acronym	SOP, PSOP
Lead Configuration	Dual-In-Line
Lead Counts	44
Lead Finish	SolderPlate
Lead Pitch	1.27mm
Board Assembly Type	Surface Mount

NOTES:
1. Alloy 42 and Cu Alloy Leads.
2. Novalac Body.
3. Bake and dessicant packaging required.

44 LEAD SMALL OUT-LINE PACKAGE (SOP)



Family: Small Out-Line Package								
Symbol	Millimeters			Notes	Inches			Notes
	Min	Nom	Max		Min	Nom	Max	
A			3.05				0.120	
A_1	0.13		0.60		0.005		0.024	
A_2	2.17	2.30	2.45		0.085	0.091	0.097	
b	0.35	0.40	0.50		0.014	0.016	0.020	
c	0.13	0.150	0.20		0.005	0.006	0.008	
D_1	27.70	28.20	28.70		1.090	1.110	1.130	
E	13.10	13.30	13.50		0.516	0.524	0.531	
e_1		1.27				0.050		
D	15.75	16.00	16.30		0.620	0.630	0.642	
L_1	0.45		0.85		0.017		0.033	
N	44				44			
Y			0.10				0.004	
θ			8°				8°	

THIN SMALL OUT-LINE PACKAGE (TSOP)

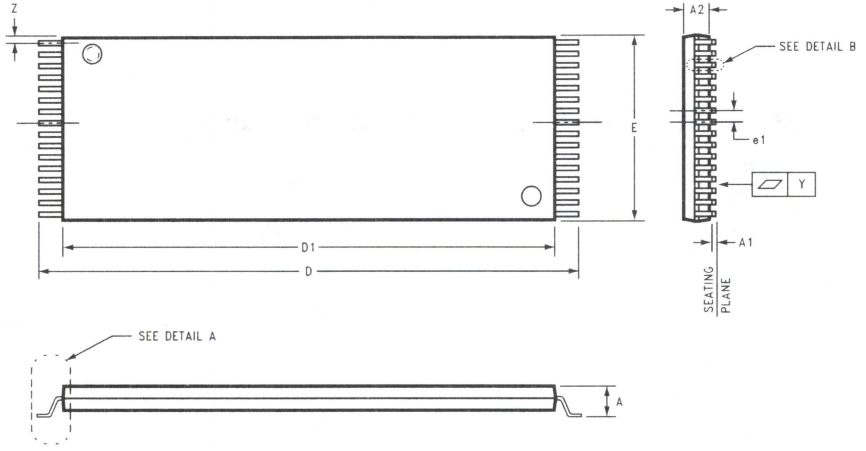
Symbol List for Thin Small Out-Line Package Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Standoff
A_2	Package Body Thickness
b	Width of Terminal Leads
c	Thickness of Terminal Leads
D_1	Plastic Body Length
E	Package Body Width
e_1	Lead Pitch
D	Terminal Dimension
L_1	Lead Foot Length
N	Total Number of Leads
Y	Seating Plane Coplanarity
Z	Lead to Package Offset
θ	Lead Tip Angle

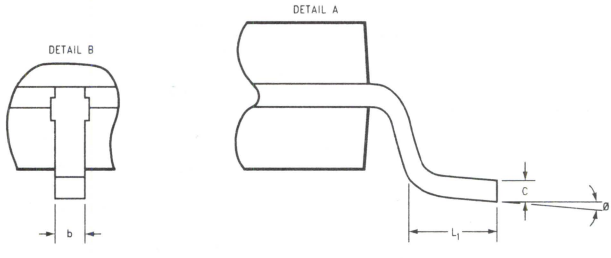
Packaging Family Attributes	
Category	Thin Small Out-Line
Acronym	TSOP
Lead Configuration	Dual-In-Line
Lead Counts	32, 40, 56
Lead Finish	SolderPlate
Lead Pitch	0.5 mm
Board Assembly Type	Surface Mount

NOTES:
1. Alloy 42 Leads.
2. Novalac Body.
3. Offered in Reverse Pin-Out for special circuit layout. (32L, 40L only)
4. Profile tolerance zones for D_1 and E do not include mold protrusion. (Allowable mold protrusion on D_1 is 0.25mm per side and on E is 0.15 mm per side.
5. Lead plating thickness is 0.007 mm–0.015 mm. (Not part of b or c dimensions)

32 LEAD THIN SMALL OUT-LINE PACKAGE (TSOP)



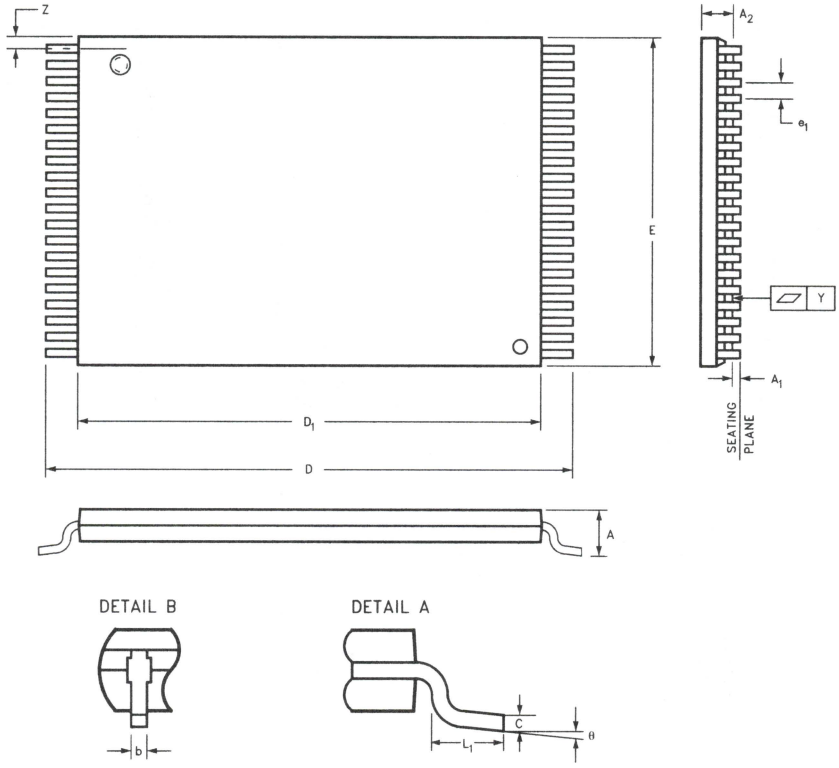
231369-64



231369-65

Family: Thin Small Out-Line Package								
Symbol	Millimeters			Notes	Inches			Notes
	Min	Nom	Max		Min	Nom	Max	
A			1.200				0.047	
A_1	0.050				0.002			
A_2	0.965	0.995	1.025		0.038	0.039	0.040	
b	0.150	0.200	0.300		0.006	0.008	0.012	
c	0.115	0.125	0.135		0.0045	0.0049	0.0053	
D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	
E	7.800	8.000	8.200	4	0.307	0.315	0.323	
e_1		0.500				0.0197		
D	19.800	20.000	20.200		0.780	0.787	0.795	
L_1	0.500	0.600	0.700		0.020	0.024	0.028	
N		32				32		
θ	0°	3°	5°		0°	3°	5°	
Y			0.100				0.004	
Z	0.150	0.250	0.350		0.006	0.010	0.014	

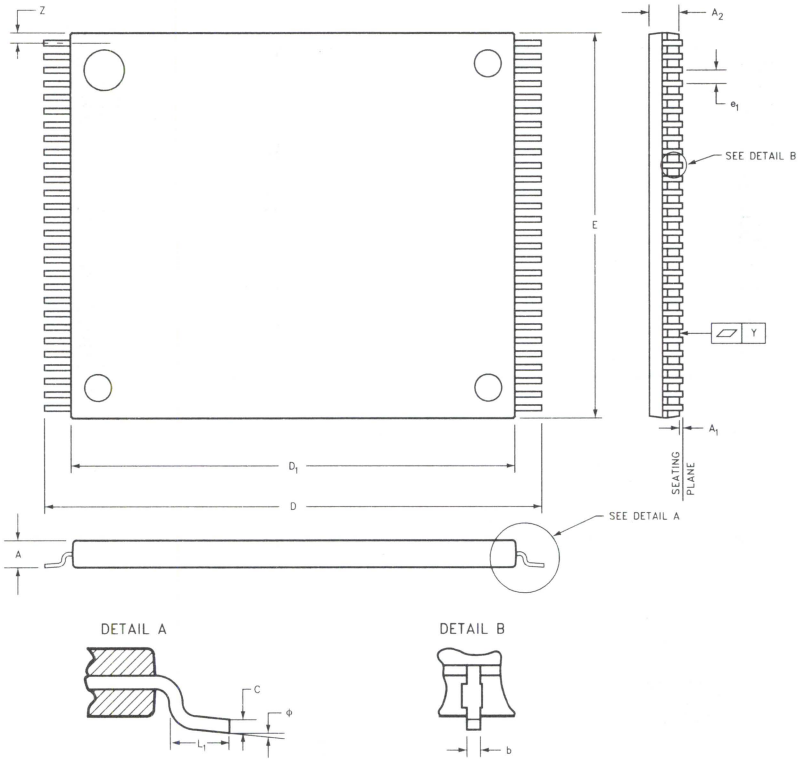
40 LEAD THIN SMALL OUT-LINE PACKAGE (TSOP)



231369-81

Family: Thin Small Out-Line Package								
Symbol	Millimeters			Notes	Inches			Notes
	Min	Nom	Max		Min	Nom	Max	
A			1.200				0.047	
A_1	0.050				0.002			
A_2	0.965	0.995	1.025		0.038	0.039	0.040	
b	0.150	0.200	0.300		0.006	0.008	0.012	
c	0.115	0.125	0.135		0.0045	0.0049	0.0053	
D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	
E	9.800	10.000	10.200	4	0.386	0.394	0.402	
e_1		0.500				0.0197		
D	19.800	20.000	20.200		0.780	0.787	0.795	
L_1	0.500	0.600	0.700		0.020	0.024	0.028	
N		40				40		
θ	0°	3°	5°		0°	3°	5°	
Y			0.100				0.004	
Z	0.150	0.250	0.350		0.006	0.010	0.014	

56 LEAD THIN SMALL OUT-LINE PACKAGE (TSOP)



231369-90

Family: Thin Small Out-Line Package								
Symbol	Millimeters			Notes	Inches			Notes
	Min	Nom	Max		Min	Nom	Max	
A			1.200				0.017	
A_1	0.050				0.002			
A_2	0.965	0.995	1.025		0.038	0.039	0.040	
b	0.100	0.150	0.200		0.004	0.006	0.008	
c	0.115	0.125	0.135		0.0045	0.0049	0.0053	
D_1	18.200	18.400	18.600	4	0.717	0.724	0.732	
E	13.800	14.000	14.200	4	0.543	0.551	0.559	
e_1		0.500				0.0197		
D	19.800	20.000	20.200		0.780	0.787	0.795	
L_1	0.500	0.600	0.700		0.020	0.024	0.028	
N		56				56		
θ	0°	3°	5°		0°	3°	5°	
Y			0.100				0.004	
Z	0.150	0.250	0.350		0.006	0.010	0.011	

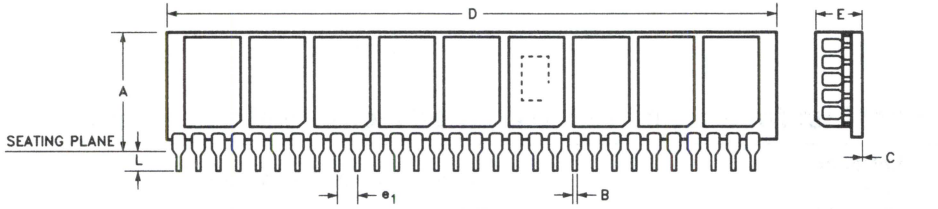
SINGLE IN-LINE LEADED MEMORY MODULE PACKAGE (SIP)

Symbol List for Single In-Line Leaded Memory Module Family

Letter or Symbol	Description of Dimensions
A	Overall Height
B	Width of Terminal Leads
C	Thickness of Terminal Leads
E	Largest Overall Package Width Dimension Outside of Leads
e_1	Linear Spacing between Centerline of Body Terminal Leads (Standoffs)
L	Distance from Seating Plane to End of Lead

Packaging Family Attributes	
Category	Single In-Line Leaded Package
Acronym	SIP
Lead Configuration	Single Row
Lead Counts	30
Lead Finish	Tin/Nickel
Lead Pitch	2.5 mm
Board Assembly Type	Socket and Insertion Mount

30 LEAD SINGLE IN-LINE LEADED MEMORY MODULE PACKAGE (SIP)



231369-67

Family: Single In-Line Leaded Memory Module (SIP)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	16.43	16.59		0.647	0.653	
B	0.557	0.559		0.018	0.022	
C	0.229	0.279		0.009	0.011	
D	78.61	78.87		3.095	3.105	
E		5.08			0.200	
e_1	2.54			0.110		
L	3.18		Typical	0.125		Typical
N	30			30		

SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)

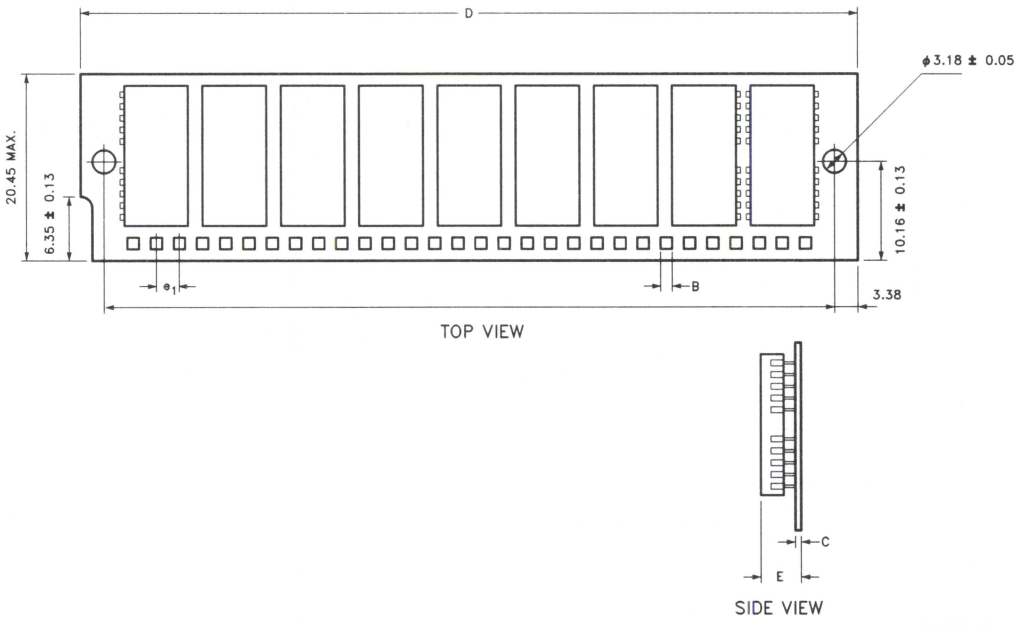
Symbol List for Single In-Line Leadless Memory Module Family

Letter or Symbol	Description of Dimensions
B	Width of Terminal Leads
C	Thickness of Terminal Leads
D	Largest Overall Package Dimension of Length
E	Largest Overall Package Width Dimension Outside of Leads
e_1	Linear Spacing between Centerline of Body Terminal Leads (Standoffs)
N	Total Number of Leads

Packaging Family Attributes	
Category	Single In-Line Leadless Memory Module
Acronym	SIMM
Lead Configuration	Single Row
Lead Counts	30, 80
Lead Finish	SolderCoat
Lead Pitch	0.100″
Board Assembly Type	Socket and Insertion Mount

NOTES:
1. Alloy 42.
2. Plastic body.

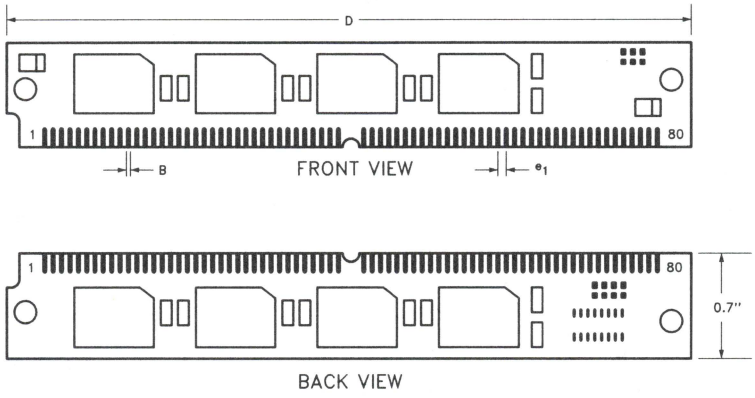
30 PIN SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)



231369-68

Family: Single In-Line Leadless Memory Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
B	1.78		Typical	0.070		Typical
C	1.19	1.40		0.047	0.055	
D	88.77	89.03		3.495	3.505	
E		5.08			0.200	
e_1	2.54		Typical	0.100		Typical
N	30			30		

80 PIN SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)

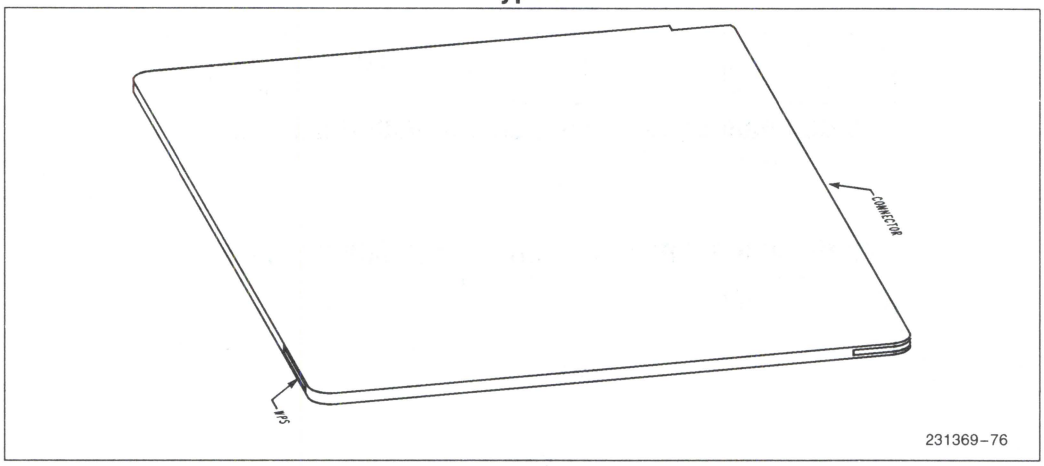


231369-69

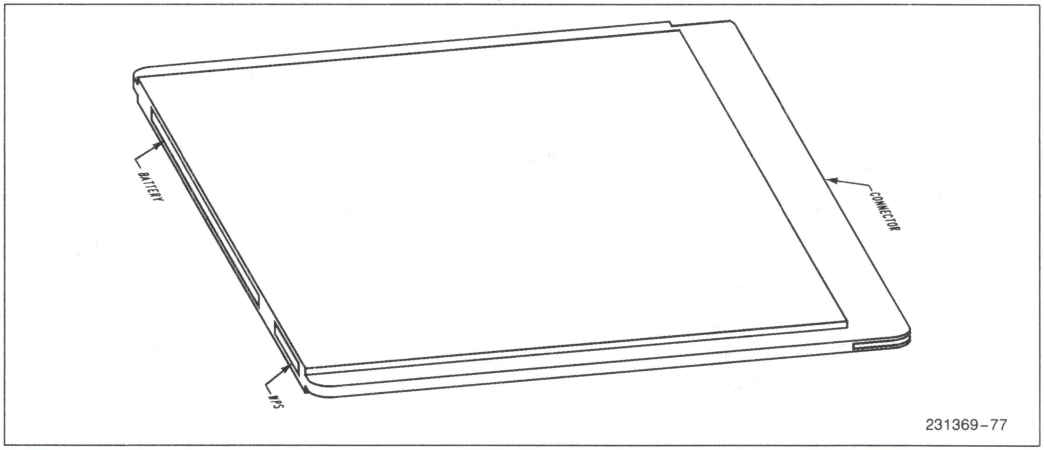
Family: Single In-Line Leadless Memory Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
B	1.04		Typical	0.041		Typical
C	1.19	1.37		0.047	0.054	
D	117.98	118.24		4.645	4.655	
E	8.38			0.33		
e_1	1.27		Typical	0.050		
N	80			80		Typical

PCMCIA PC CARD TYPE I AND TYPE II

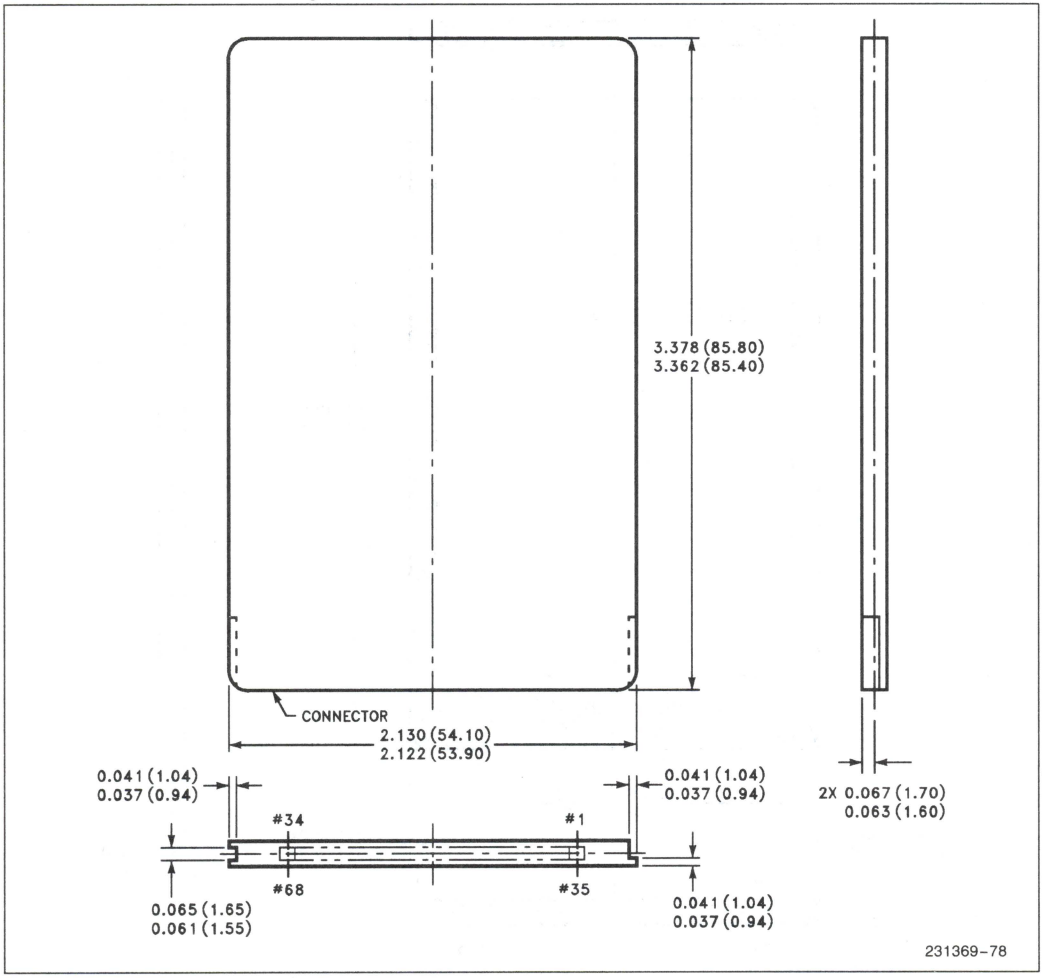
Type I



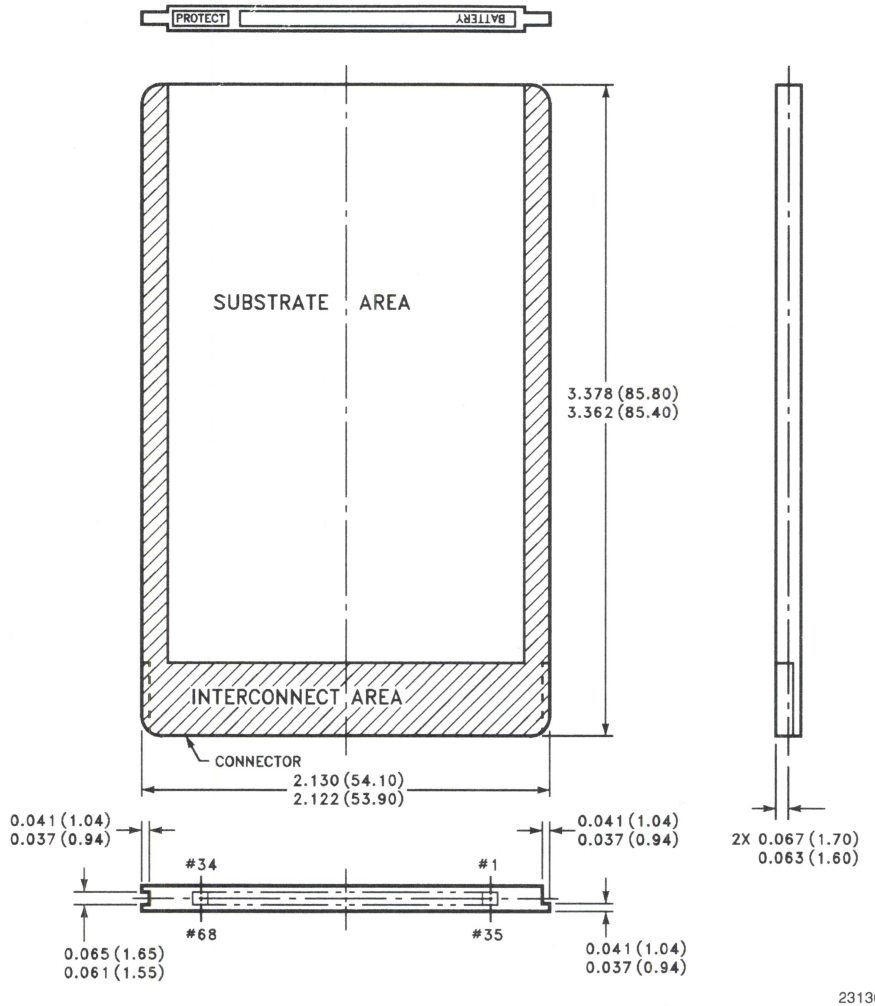
Type II



Type I PC Card Package Dimensions



Type II PC Card Package Dimensions



PC Card Physical Dimensions

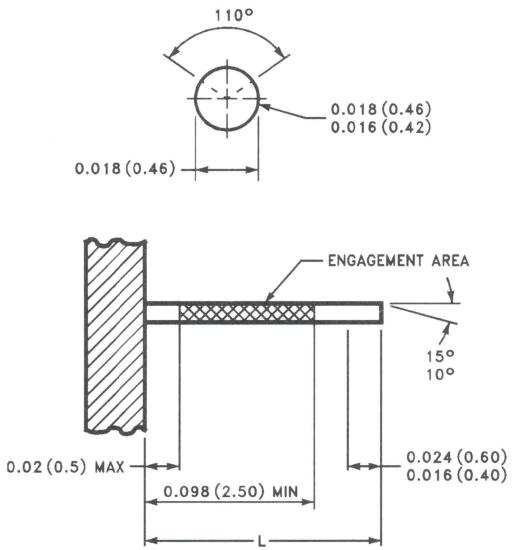
	Length	Width	Interconnect Area(1)	Substrate Area (1)
Type I	3.370 ±0.008 (8.56 ±0.20)	2.126 ±0.004 (54.0 ±0.10)	0.65 ±0.002 (1.65 ±0.06)	0.65 ±0.002 (1.65 ±0.06)
Type II	3.370 ±0.008 (85.6 ±0.20)	2.126 ±.004 (54.0 ±0.10)	.065 ±0.002 (1.65 ±0.06)	0.098 (2.5) Max

NOTES:
1. Interconnect area and substrate area thickness are specified from the IC memory card center line to either the top or bottom surface.
2. Millimeters are in parentheses ( ).

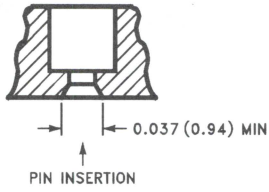
Host Connector Pin Configuration for Both Type I and Type II

Pin Type	Pin Length (L)	Pin #
Detect	0.142 (3.6) 0.134 (3.4)	36, 67
General	0.171 (4.35) 0.163 (4.15)	All Other Pins
Power	0.201 (5.1) 0.193 (4.9)	1, 17, 34, 35, 51, 68

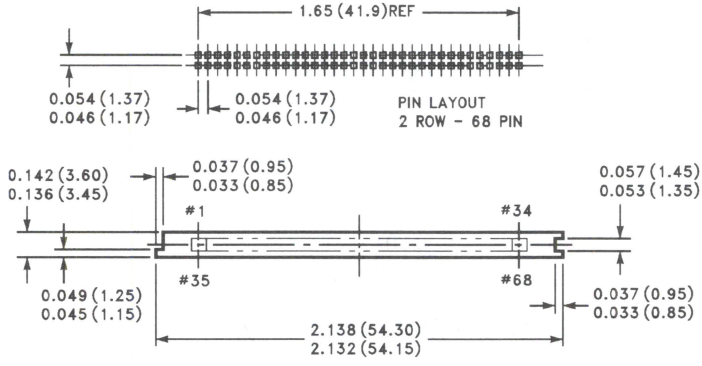
PC Card Contact Pins for Both Type I and Type II



PC Card Connection Socket for Type I and Type II



PC Card Connector for Type I and Type II



REVISION SUMMARY

The main differences between rev 010 and rev 009 are the following:

- Deleted LGA
- Deleted ZIP
- Revised PGA Dimensions
- Revised PSOP and TSOP Dimensions
- Revised QFP, SQFP andd TQFP Dimensions

IC Assembly Technology 3

CHAPTER 3
IC ASSEMBLY TECHNOLOGY

INTRODUCTION

The material and process technology steps used to manufacture or assemble Intel's three basic types of component packages differ only in detail.

The package families, described in Chapter 1, provide the functional specialization and diversity required by our customers. Material and construction attributes of individual family members are provided by the following package technologies: (1) laminated ceramic, (2) pressed ceramic, and (3) molded plastic.

As shown in Table 3-1, not all combinations of package families (form, fit, function) and package assembly technologies are available.

Figure 3-1 illustrates the package assembly steps common to the three basic package technologies. The descriptions of Intel assembly technologies that follow are arranged in sequence of these process steps, and are preceded by a description of the statistical methods used throughout process development to ensure a reliable, high-quality, manufacturable product.

Table 3-1. Intel Package Families and Technologies

Package Family	Package/Assembly Technologies		
	Single Layer		Multilayer
	Pressed Ceramic	Molded Plastic	Laminated Ceramic
Dual In-Line Pin (DIP)	X	X	X
Chip Carrier:			
Leadless			X
Leaded	X	X	X
Pin Grid Array			X

STATISTICAL TOOLS IN ASSEMBLY TECHNOLOGY

Statistical tools are critical to achieving the high yields and extremely low defect levels required in today's competitive component manufacturing environment.

As shown in Figure 3-2, new Intel processes undergo three development phases using a wide variety of statistical tools prior to production:

- Feasibility demonstration
- Process characterization
- Manufacturing validation

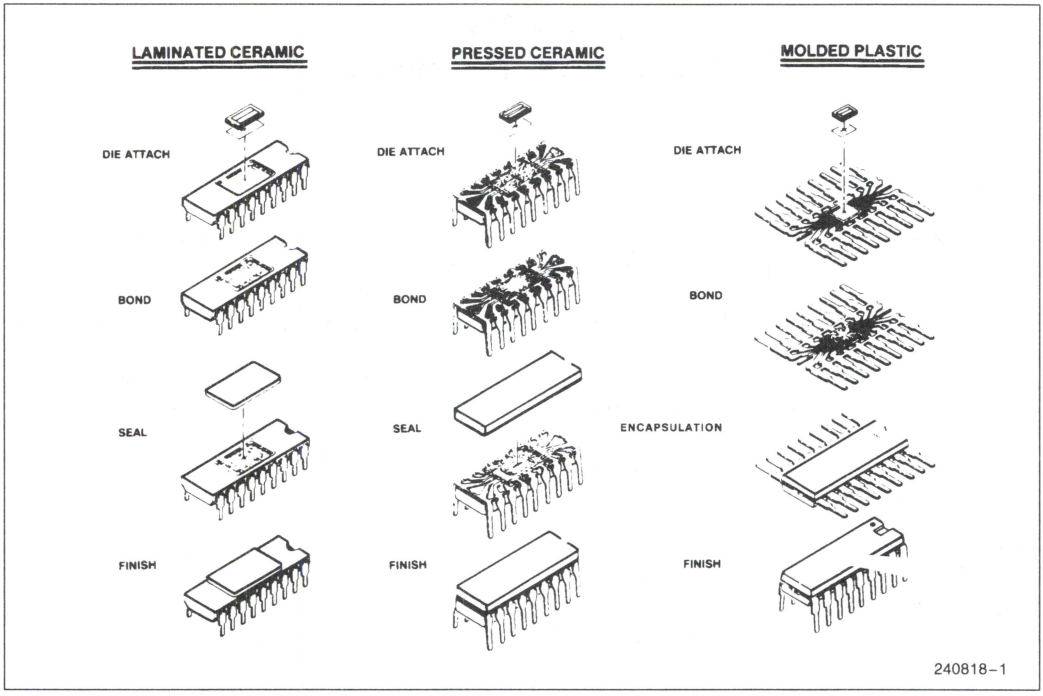


Figure 3-1. Generic Package Technologies—Process Steps

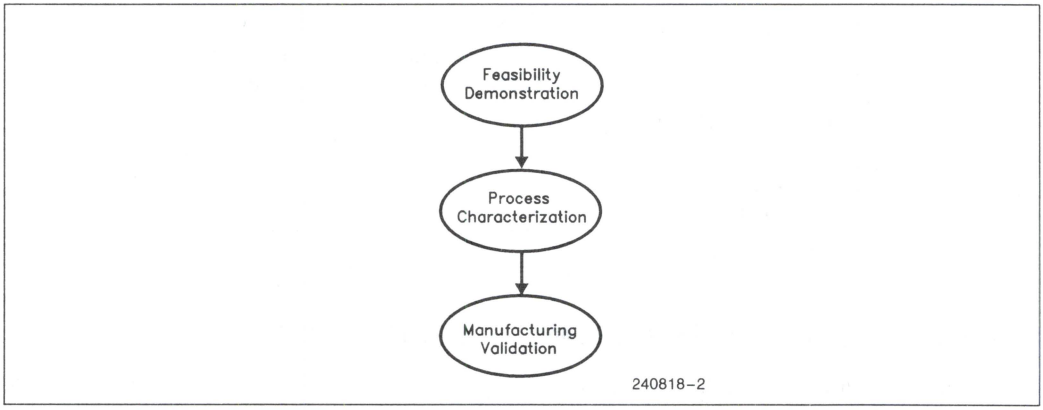


Figure 3-2. Development Statistical Methods Model

Feasibility Demonstration

At this stage of development, Intel engineers use small laboratory experiments to determine the manufacturability of a new process. Obvious design flaws and process difficulties, as well as areas in which the process differs significantly from expectations, are identified during feasibility demonstration.

The most valuable statistical tools used to determine feasibility are simple graphical techniques, including scatter plots, histograms, boxplots, and bar graphs. While data may be insufficient to represent the process variation fully, plotting of the data provides the insight necessary for making critical decisions on the process.

Process Characterization

During this phase, Intel engineers characterize process performance by determining how all important input variables to the process (e.g., temperature and material characteristics) affect the response or output variable of the process to be measured, such as bond line thickness, adhesion, package moisture content, and package reliability under environmental stress.

Process characterization makes extensive use of systematic design of experiments (DOE) methodology. In planning experiments, DOE allows consideration of all important input and output variables and includes such techniques as randomization, replication, and blocking. A common type of experiment is the factorial design, in which combinations of factors are changed systematically to learn how factors interact to affect a specific response.

In the early development phases of a new process when there is usually a wide range of variables to consider, Intel engineers study a fraction of the many combinations of variables possible, thus conserving resources. These experiments are known as fractional factorial designs or screening designs. As more is understood about a process, some variables may be set constant at optimum levels, while others continue to be investigated and refined in follow-up experiments. This "phased experimentation" approach systematically identifies and modifies variables until the critical process parameters have been determined and an optimum operating window has been established.

Often during the process characterization stage, Intel engineers must develop the metrology for a given process. In this case, a measurement capability study is a useful tool for ensuring that the measurement process can provide the precision required.

Another key statistical tool useful in the characterization phase is the process capability study. During these studies, Intel engineers use control charts such as the one shown in Figure 3-3 to monitor critical process parameters at regular intervals and examine process stability over time.

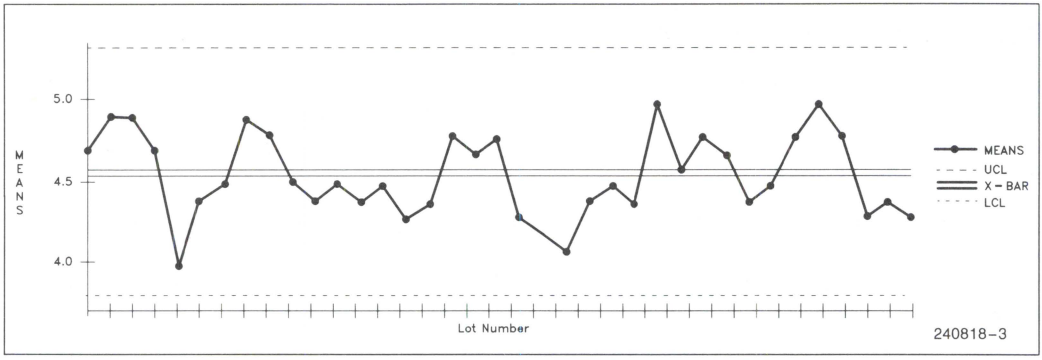


Figure 3-3. X-Bar Control Chart, Bond Line Thickness (mils)

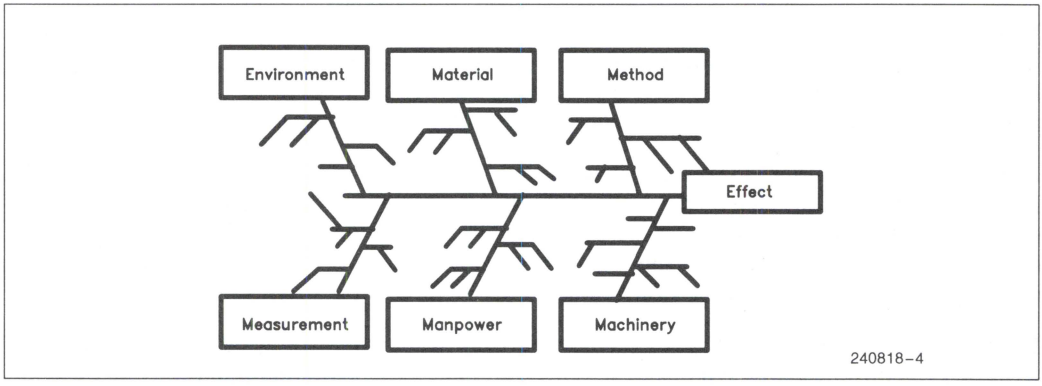


Figure 3-4. Cause/Effect Diagram

As shown in Figure 3-4, problem-solving tools such as cause-and-effect (fishbone) diagrams and process flow charts are useful in all stages of process development and are invaluable during the design of an experiment.

Manufacturing Validation

During the manufacturing validation stage, the process is piloted at Intel's engineering development line where processes/products are engineered and fully characterized before introduction to assembly production lines. At this time, results of the characterization are verified using production equipment, and other necessary experiments are performed. The process remains in the validation stage until it is proven and accepted as cost-effective, manufacturable, high-quality, reliable process.

DIE PREPARATION

Intel protects the surface of silicon devices from handling-induced defects by using contactless handling throughout wafer processing, die singulation, and the separation of dies from the wafer.

Wafer preparation for sawing is also contactless, from wafer mounting and application of supporting tape (by balanced air-pressure technique) to the sawing operation itself. Intel uses through-wafer sawing to eliminate surface contact during die separation and follows with a high-pressure DI (deionized water) wafer wash to eliminate particulate contamination.

In addition, special care is taken to minimize surface contact in all subsequent assembly process steps.

DIE ATTACH

Intel die attach materials fall into two categories: (1) adhesives, both organic and inorganic; and (2) hard solders (gold-silicon eutectic). The choice of die attach materials depends on the specific applications and is compatible with the particular packaging technologies to ensure the highest levels of performance and reliability. Table 3-2 summarizes the die attach materials used at Intel by package type.

Table 3-3 is a summary of the properties of die attach materials used at Intel.

Table 3-2. Die Attach Materials by Package Type

Package	Die Attach Material	Type
Pressed Alumina Ceramic (CERDIP, Cerquad)	Silver-Filled Glass	Inorganic Adhesive
Laminated Alumina Ceramic (PGA, CQFP, Side-Braze)	Gold-Silicon Eutectic Silver-Filled Cyanate Ester	Hard Solder Organic Adhesive
Molded Plastic (Alloy 42 Lead Frame)	Silver-Filled Polyimide	Organic Adhesive
Molded Plastic (Copper Lead Frame)	Silver-Filled Epoxy	Organic Adhesive

Table 3-3. Die Attach Material Summary

	Au-Si	Silver-Filled Glass	Silver-Filled Polyimide	Silver-Filled Epoxy/Cyanate Ester
Wafer Backside Metallization for Die Attach	Required	Not Required	Not Required	Not Required
Wafer Backside Metallization for Ohmic Contact	Not Required	Required	Required	Required
Thermal Dissipation	Good	Good	Fair	Fair
Electrical Conductivity	Good	Good	Fair	Fair
Lead Frame Compatibility (a) Alloy 42 (b) Cu Alloy	 N/A N/A	 N/A N/A	 Good Poor	 Good Good
Substrate Metallization Compatibility (a) Gold (b) Silver (c) Al_2O_3	 Good Good N/A	 Poor Good Good	 Good Good N/A	 Good Good N/A

Figures 3-5 through 3-8 are schematic cross-sections through each of the different die attach systems currently in use at Intel, i.e., gold/silicon eutectic, silver-filled glass, and silver-filled organic adhesives, polyimide, epoxy, and cyanate ester. The components of each system are identified.

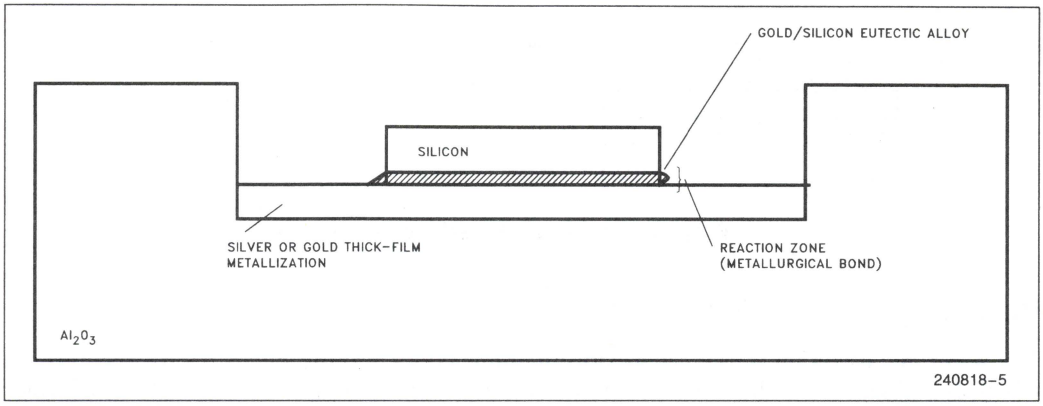


Figure 3-5. Gold-Silicon Eutectic

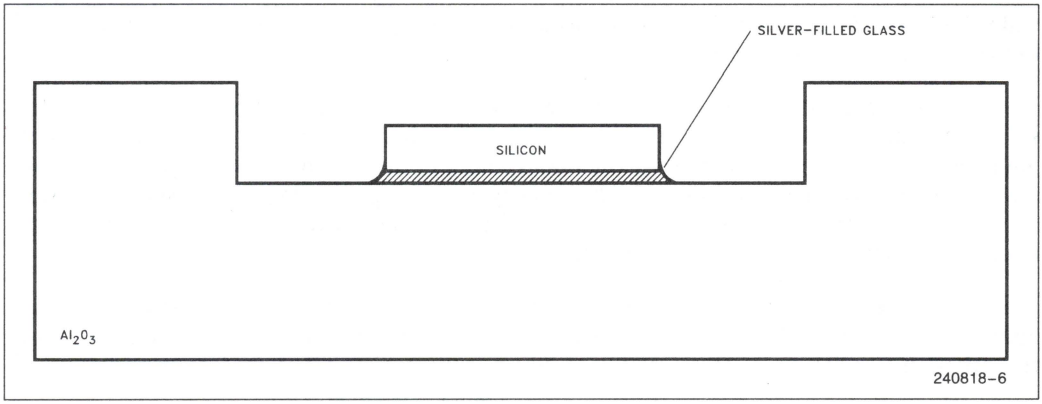


Figure 3-6. Silver-Filled Glass

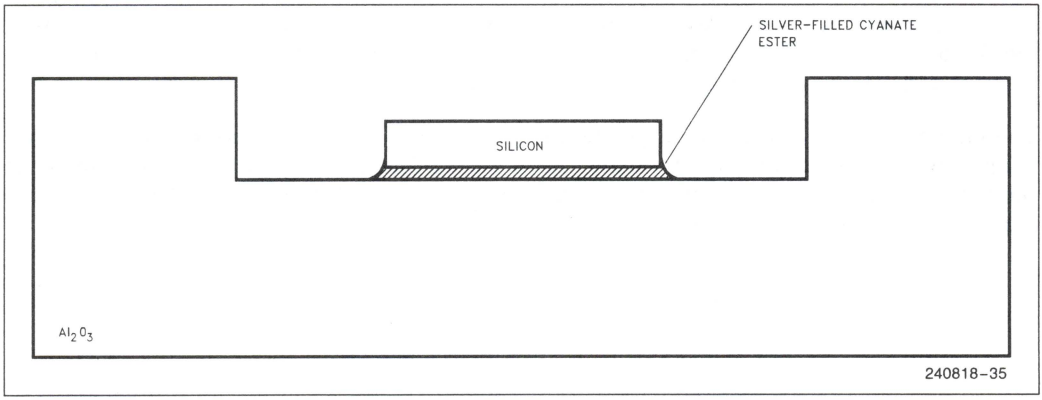


Figure 3-7. Silver-Filled Cyanate Ester

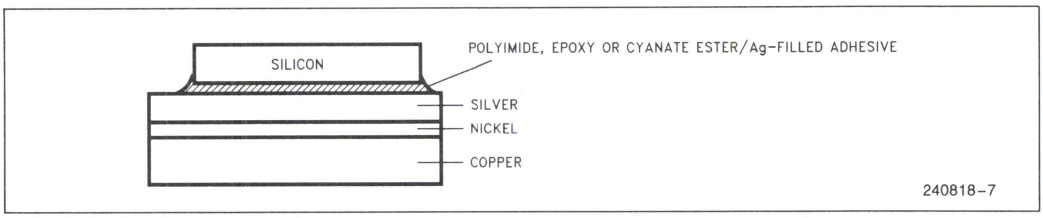


Figure 3-8. Silver-Filled Adhesive

Purpose of Each Component

The **wafer metallization** is used to provide an ohmic contact to the silicon die for the purpose of substrate biasing for those die attach media that do not readily form any ohmic junction, i.e., silver-filled glasses, epoxies, polyimides, and cyanate ester. It provides a readily wettable surface for gold/silicon hard soldering and prevents premature oxidation (or aging) of the wafer backside during storage by acting as a diffusion barrier, thus ensuring that die attach integrity remains uncompromised.

Like the wafer backside, the **substrate metallization** is used to provide a readily wetted surface for hard soldering. The metallizations used in hermetic package technologies, both gold and silver, are readily wetted by the liquid solder at die attach temperatures and actually react with the solder to provide a high-integrity metallurgical bond to the substrate. Both substrate metallizations resist oxidation, which can impede wetting, and are electrically conductive for those devices that require electrical contact.

Plastic packages use a plated silver metallization that is wetted by and adherent to organic adhesives, and that is electrically conductive. Silver-filled glass does not require a metallization, though it will adhere quite readily to silver.

The **die attach media** themselves serve several purposes other than the obvious one of attaching the silicon to the substrate. They also provide a means of making an electrical connection to the die backside for those devices requiring it, as well as a path for conduction of heat from the die to the ambient. For these reasons, the die attach media used at Intel exhibit good thermal and electrical conductivity.

The incoming quality of die attach materials is monitored through a series of specifications unique to each of the die attach media. Tests are performed at Intel and by our material vendors to measure those specific characteristics necessary to ensure that materials meet the requirements of die attach applications.

Process Limitations

From the standpoint of process design, it is necessary to understand the limitations of each die attach process. Each of the die attach technologies used at Intel has its own limitations with an impact on applications.

Au-Si EUTECTIC

There are three key limitations to this process. Foremost is the effect of processing temperature on die reliability and performance; it is necessary to design silicon fabrication processes so that they can withstand the Au-Si process temperatures for the die attach duration. Next is the need for die backside metallization for even moderate die sizes and for those applications demanding the highest reliability. All Intel dies use a wafer backside metallization. The third limitation is the need for excellent process control. This limitation is discussed in a later section.

SILVER-FILLED GLASS (SFG)

SFG, like Au-Si eutectic, is limited to those devices that can withstand the SFG processing temperature and time. Again, the silicon fabrication processes need to be designed to withstand the die attach process. Because of the organic content (solvent and resin binder) of the SFG paste, there are limits on the minimum dry times versus die size that constrain the process. Larger dies mean longer drying/processing times.

There are also limits to the bond line thickness, both thin and thick, that constrain the process. In addition, it is imperative to maintain a nearly void-free die attachment. SFG is limited to (1) nongold wafer backsides and substrates due to poor adherence to gold, and (2) inert or oxidizing processing ambients.

Like Au-Si eutectic, SFG requires close process control. Once processed, the SFG material is stable to extremely high temperatures.

SILVER-FILLED POLYIMIDE

Like SFG, the silver-filled polyimides contain a significant volume of solvent that must be carefully removed during processing to minimize voiding. Also, water vapor is released during the imidization reaction and must be carefully removed to prevent voiding.

Because of these considerations, the polyimide process must be designed properly, allowing long processing times for large dies. As die size increases, processing times may become prohibitive from a manufacturing point of view. Because of the large volume changes (shrinkage) associated with the solvent loss, die attach stress occurs; in most applications, however, this is not a concern, since the stresses tend to be compressive. However, with copper lead frames, the stress can increase to a point where the frames are damaged during processing, especially with larger dies. There is a minimum bond line thickness limitation for polyimide, below which stresses on the die can increase.

Polyimide adhesives are stable to very high temperatures and are not affected by temperature exposure during subsequent processing. The polyimide material used at Intel is stable to at least 450°C for short periods of time.

SILVER-FILLED EPOXY/CYANATE ESTER

There are two significant limitations on these adhesives. The first is the upper temperature that the material can tolerate before decomposition occurs, which is approximately 200°C for epoxy and 380°C for cyanate ester. The second is a limitation on the minimum bond line thickness, again a die stress concern. As with the other paste technologies, it is important to maintain a nearly void-free die attachment through control of the dispensed paste volume.

Processes

Au-Si

Figure 3-9 is a representation of the gold-silicon phase diagram. In this process, a pure gold preform is placed into a preheated ceramic package under a heated inert gas. The die is placed onto the preform and allowed to reach the preset die attach temperature.

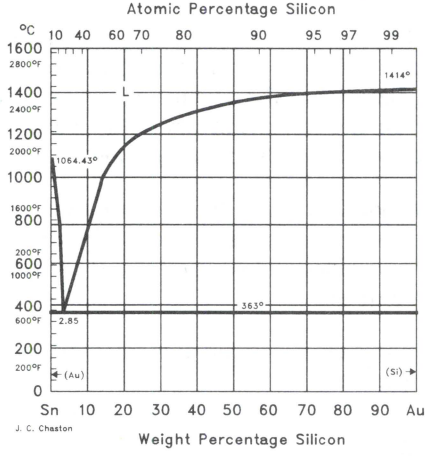


Figure 3-9. Au-Si Gold-Silicon

As the temperature is raised, silicon from the die begins to diffuse through the diffusion barrier on the die backside, and at 363°C, forms eutectic composition liquid. Once liquid formation occurs, the reactions proceed rapidly by liquid phase diffusion. As the temperature increases beyond the eutectic temperature, more silicon is dissolved from the die backside until the equilibrium volume of silicon is reached. The liquid also begins to dissolve the gold or silver substrate. The amount of gold or silver that dissolves depends on the temperature and the time of die attach.

At this point, a circular motion is used to distribute the liquid evenly across the silicon backside to ensure intimate contact with all areas. Once this is accomplished, the package and die are cooled. During cooling, silicon begins to precipitate from the saturated gold-silicon liquid. These precipitates grow epitaxially from the silicon die backside. Analysis using a transmission electron microscope has confirmed that the epitaxial region is continuous with

the bulk silicon crystal structure. When the package again reaches the eutectic temperature, the solder solidifies with a characteristic eutectic-type microstructure. There is no solid solubility of silicon in gold or vice versa, as evidenced by the phase diagram for the system. The joint obtained upon cooling is metallurgically continuous from the substrate to the die.

SILVER-FILLED GLASS

Silver-filled glass is a suspension of silver and low-softening temperature glass particles in an organic vehicle. In this process, the paste is automatically applied to the ceramic via a paste dispense system. After the paste is applied, the die is positioned within the dispensed pattern. Because of the high organic content of the paste, the SFG is carefully dried in a continuous furnace to remove the solvent. This leaves behind a resin that binds the silver and glass particles until subsequent processing can soften the glass. After drying, the material is carefully heated to remove the binder; the heating rate is determined by die size.

At higher temperatures, the glass begins to soften, and the silver particles begin to sinter together into a cohesive mass. Considerable shrinkage accompanies the reactions at higher temperatures, and care must be taken to ensure that the minimum bond line thickness requirements are maintained after shrinkage. At the highest temperatures, the glass wets the silver particles, silicon surface, and ceramic substrate, creating a strong chemical bond between the silicon and the ceramic. Once the material has reached the maximum density, the package is cooled and readied for subsequent assembly operations.

SILVER-FILLED POLYIMIDE

The processing for silver-filled polyimide, because it is a solvent-filled system, is similar to that of silver-filled glass. The paste is dispensed and the die positioned on automatic equipment similar to that used for SFG. Once again, it is necessary to remove the solvent from the system in a drying step prior to the imidization reaction. The drying operation is again dependent on die size (diffusion length) and has been designed to be compatible with all die sizes.

After drying, the polyimide is raised in temperature to initiate the imidization reaction. This reaction generates water vapor, and thus care must be exercised to ensure that the water is fully removed during the process. Like drying, this operation depends on die size and has been carefully designed to maximize water vapor desorbtion.

At the highest processing temperatures, the polyimide fully cures and forms a strong chemical bond to the lead frame and silicon. At this point, the package is cooled and sent to the subsequent assembly operation.

SILVER-FILLED EPOXY/CYANATE ESTER

The silver-filled epoxy/cyanate ester used by Intel is a so-called solventless system, which eliminates the processing issues associated with drying. Because of the chemical structure of these adhesives, water vapor evolution during process is also not a concern. As with the other paste technologies (polyimide and SFG), the paste is automatically dispensed and the die positioned on automated equipment, with care taken to ensure a void-free die attach. After placement, the package is heated to the epoxy resin cure temperature to polymerize the epoxy/cyanate ester and create the final chemical bond between the silicon and lead frame or substrate.

BACKSIDE REQUIREMENTS AND CONTROLS

The wafer backside process can have an effect on the integrity of the joint created during die attach. From gold-silicon eutectic work, Intel has determined that a metallized surface is required for highly reliable joining. The quality of the metallization modulates the wetting of the liquid to the silicon and enhances the quality of the braze joint. It has also been determined that the roughness of the surface plays a significant role in eutectic die attach, and that smooth surfaces wet more readily and more quickly than rougher ones.

Because there is a need to prevent premature oxidation of the metallization, a diffusion barrier is necessary. The barrier is required to adhere to both silicon and gold, yet not interfere with the integrity of the final joint. Finally, the barrier kinetics also must allow rapid diffusion of silicon at the die attach temperatures. Because of this, it is necessary to control the thicknesses of the barrier metal. The gold thickness must also be controlled to prevent oxidation of the barrier metal.

OHMIC CONTACT

Some MOS devices require an ohmic contact to the die backside. To achieve an ohmic contact, a metallization is required for all of the paste technologies, as the silver will not form a low-resistance ohmic contact at any of the die attach times or temperatures. An ohmic contact can be achieved with gold-silicon eutectic die attach without the use of a metallization, as the gold readily diffuses at the die attach temperature, creating a low-resistance contact. However, in Intel's experience, a wafer backside metallization is necessary for the creation of a highly reliable eutectic joint.

Performance and Engineering Characteristics

DIE SIZE LIMITATIONS

- **Au-Si.** At this time, there are no known limits to the die size that can be attached with this technique. Dies as large as 1.8 x 1.8 cm (0.7 x 0.7 in.) have been successfully attached by this technique.
- **Silver-Filled Glass.** It has been demonstrated that dies as large as 1.0 x 1.0 cm (0.4 x 0.4 in.) can be successfully attached by this technique.
- **Silver-Filled Polyimide.** It has been demonstrated that dies as large as 1.0 x 1.0 cm (0.4 x 0.4 in.) can be successfully attached by this technique.
- **Silver-Filled Epoxy/Cyanate Ester.** Because there are no limitations on solvent or water vapor evolution for this type of paste, there are no known die size limitations. Dies as large as 1.3 x 1.3 cm (0.6 x 0.6 in.) have been successfully attached using this die attach material.

JOINT STRENGTHS

Table 3-4 summarizes the die attach joint strengths and typical failure modes for each of the die attach materials used at Intel today. As shown, measured strengths easily exceed the military specifications for die attach strength as determined by tensile testing.

A typical failure mode for Au-Si is fracture of the silicon. For the other technologies, failure of the adhesive material, i.e., a cohesive failure, is typical.

Table 3-4. Typical Tensile Bond Strengths of Various Die Attach Media

Die Attach Media	Tensile Strength (kg/cm^2)	Tensile Strength (psi)
Au-Si	500	>7000
Silver-Filled Glass	100	1400
Silver-Filled Polyimide	140	2000
Silver-Filled Epoxy	140	2000
Silver-Filled Cyanate Ester	140	2000

MODELING RESULTS

Modeling conducted at Intel has shown that die cracking during temperature cycling can be caused by stress risers in the die attachment. While small voids in the die attachment act as stress risers, they do not create the type of tensile forces necessary to fracture silicon. Only when voids occur at die corners or edges do tensile stresses result that can cause the silicon to fail. Typically, edge voids in Au-Si are the result of improper wetting of the liquid to the silicon surface, which causes the liquid to take up a lower surface energy configuration, and pulling away from the die edge. Subsequent temperature cycling creates a tensile stress at the void/solder interface that fractures the silicon. Proper metallization techniques minimize this risk by preventing dewetting during die attach.

The same effects can occur with the paste technologies during die attach. Therefore, it is imperative to maintain a void-free die attach, particularly edge voids. Care is taken during paste dispense to ensure that the entire die area is fully covered by die attach media to minimize the risk of edge void formation.

BACKSIDE METALLIZATION CONTROLS

Control of the wafer backside metallization process is essential for high-integrity gold-silicon eutectic bonds. As mentioned, it is important to control the thicknesses of both the barrier metal and the gold. It is also necessary to control the deposition conditions to minimize the oxygen content of the barrier metal. Failure to do so can result in a poorly wettable surface that does not allow rapid, uniform silicon diffusion at the Au-Si die attach temperatures.

WIRE BONDING

Wire bonding is an assembly step that connects the input/output of the device to the package terminals. At this stage in the assembly process, the majority of the final cost is already in the device. Thus, it is critical that the highest yield of wire bonding is achieved.

To ensure a high-quality, reliable wire bond, Intel engineers have made significant advances in techniques to control and monitor the bonding process.

Wire-Bonding Techniques

Intel wire-bonding techniques include (1) thermosonic, or gold ball bonding; and (2) ultrasonic, or aluminum wedge bonding.

In thermosonic bonding, a gold ball is formed at the end of the wire, and a bond is made between the bond pad surface and gold ball. With the ultrasonic bonding technique, a bond is made directly between the wire and the bond pad.

Bonding Parameters

Key bonding parameters include machine, material, and structural parameters. To achieve a high-quality wire bond, bonding parameters must be well understood and controlled.

The most important **machine parameters** are force, ultrasonic energy, temperature, and time. Controlling the interaction of these parameters is critical to bond quality and reliability.

Force is applied to establish and maintain an intimate contact between wire and metal surfaces during application of ultrasonic energy.

Ultrasonic energy is used to reduce the level of applied stresses necessary for plastic deformation of wire and metal surfaces by generating a larger number of mobile dislocations.

Heat (thermal energy) is applied in thermosonic bonding to compensate for ultrasonic energy attenuation by gold ball and ultrasonic reflection at the interface of ball and bond pad metallization. Applied thermal energy helps to reduce the level of stresses necessary for plastic deformation of substrate metallization.

Finally, the function of the parameter time is to control the amount of plastic deformation at the gold ball/pad metallization interface for bonding.

A number of **material and structural parameters** also have significant impact on the quality and reliability of the wire-bonding process and are strictly controlled. Intel works closely with wafer fab process development teams and our wire and lead frame vendors to obtain required characteristics for wire, metal surfaces, and structural parameters.

Critical parameters for wires are diameter, tensile strength, elongation, composition, and surface contamination.

For metal surfaces, controlled parameters include surface hardness, roughness, cleanliness (freedom from glass residues, oxide, silicon dust), and structural parameters.

Key structural parameters include (1) shape and dimensions of bonding surfaces (bond pad and lead tip); (2) number, thickness, and mechanical properties of underlayer materials; (3) integrity of underlayer interface (adhesion of underlayer materials); and (4) material interactions among wire-bonding elements, such as interdiffusion and intermetallic compound formation.

Bonding Process Quality Tools

To achieve high-quality wire bonds, Intel precisely measures and optimizes all bonding parameters. A number of techniques and bonding process quality tools have been developed for measuring the parameters of force, ultrasonic energy, time, and temperature, and have contributed significantly to improved bond quality and reliability.

FORCE MEASUREMENT

It is essential to measure the actual force applied to wire and metal surfaces—the work piece—during bonding. The applied force usually consists of two distinct elements: dynamic and static components. To measure the actual force applied to the work piece during the bonding cycle, Intel uses a dynamic force measurement system (DFM). The heart of the system is a very fast-response transducer with extremely high sensitivity to small force changes of ± 1 gram. The DFM system allows Intel to measure the actual applied force in real time. With this technique, we can identify the following:

- Actual bond force duration and amplitude
- Dynamic and static portions of the force curve
- Repeatability of applied force from one bond to another
- Machine-related problems affecting the force curve
- Timing for the application of ultrasonic energy as compared to the force curve
- Methods for duplicating the optimized force from one machine to another

Another important bonding parameter is time, which controls the level of plastic deformation in wire and substrate metallization. During the selected time, ultrasonic energy and force are applied to the wire and substrate. The application of ultrasonic energy to the work piece at the desired time, during the application of force, is called the timing factor. This parameter ensures consistent bond quality and reliability. The timing factor can be adjusted using the DFM unit.

ULTRASONIC MEASUREMENTS

To obtain optimum wire-bonding results, Intel continually measures the amount of ultrasonic energy applied to the wire or substrate.

A laser interferometry system and a special tool that precisely gauges the amount of displacement of the bonding tool tip are used for these measurements. As a result, we can perform the following with a high degree of accuracy:

- Measure the amount of ultrasonic energy
- Duplicate the optimum values on other bonders
- Inspect the machine set-up
- Inspect all incoming transducers for efficiency
- Detect defective transducers or inadequate mechanical coupling

TEMPERATURE MEASUREMENTS

Another major bonding parameter is thermal energy, which is applied to the substrate. An incorrect bonding temperature can result in a number of bonding problems. For example, high temperature can result in softer bond pad metallization, which causes metal splash and bond pad fracture. A temperature that is too low can result in harder metallization and consequently prevent materials from sticking.

Using an infrared monitor system instead of thermocouple, Intel can measure the exact temperature of bonding surfaces. We can also identify any design or material-related problems in our heater block system. As a result, we have achieved superior control of our bonding process.

Bond Quality Monitors

Intel uses a variety of techniques for measuring the quality and reliability of bonds. The most frequently used techniques are:

- Visual inspection
- Bond pull
- Shear test
- Infrared microscopy
- Bond etching
- Electrical testing
- Bake test
- Thermal cycle/thermal shock testing

VISUAL INSPECTION

Visual inspection is used to determine bond quality problems such as smashed bonds, skinny bonds, misplaced and deformed bonds, as well as wire conditions. It also determines metal surface conditions, including corrosion, cracks, voids, contamination, and extent of plastic deformation.

BOND PULL

The bond-pull strength test is a primary method used by Intel for optimizing the bonding window schedule and quality. The pull test is a relative test for a particular package configuration. Test results include bond strength and mode of failure.

SHEAR STRENGTH

Intel optimizes bond schedule by using the shear strength test, which is independent of wire condition and measures bond strength. The failure mode and bond strength are used as measures of bond quality and reliability.

INFRARED MICROSCOPY

Intel uses the reflective infrared microscopy (IR) technique to inspect the integrity of bond pad structures. This technique eliminates the need for decapping and accessing the die surface.

ELECTRICAL TESTING

Electrical testing measures the increase in ohmic resistance of bonds as a result of intermetallic compound and void formations, thus determining the effect of different materials and bonding process parameters on bond reliability.

BOND ETCHING

Bond etching measures the condition of layers under the bond pads. With this technique, the ball (wire) and pad metallization is removed, and the condition of underlayer materials is examined. Bond etching is useful for determining the weakest link in underlayer materials by identifying the initiation and propagation of cracks in underlayer materials.

BAKE TEST

Bake test measures the effect of intermetallic compound formation and Kirkendall voiding at wire/metal surface interfaces on bond reliability.

THERMAL CYCLE/THERMAL SHOCK TESTING

Thermal cycle and thermal shock testing are used to accelerate any possible bond pad fracture, bond lifting, and metal lifting due to bonding process deficiency or package configuration.

SURFACE ANALYSIS

Surface analysis techniques such as energy-dispersive X-ray analysis (EDX), wave-length dispersive X-ray analysis (WDX), Auger, and scanning electron microscopy (SEM) are the tools Intel uses to identify (1) the presence of contamination, (2) extent of intermetallic compound formation, and (3) bond irregularities. These techniques are part of our routine monitors of material parameters and failure analysis.

PLASTIC MOLDING

Advances in the technologies of molding compound chemistry and formulation, transfer molding, and package design have made it possible for Intel to manufacture highly reliable plastic component packages. Molded plastic packages have, in fact, gained a significant share of the devices we currently sell.

Composition

Molding compound is a composite material, with each component providing a set of properties critical to the overall performance of the system.

The composite matrix material used in Intel packages is an epoxy cresol novolac polymer. This crosslinked material is dimensionally stable, ionically clean, and resistant to assembly process and field-use temperatures. The composite's largest component by weight is silica filler, added to provide control of thermal expansion coefficient and thermal conductivity.

The balance of the compound consists of elastomeric toughening fillers, flame retardants, coupling agents to improve adhesion between matrix and filler, and release agents to allow removal of the product from the mold. Figure 3-10 is an electron micrograph showing the epoxy molding compound structure.

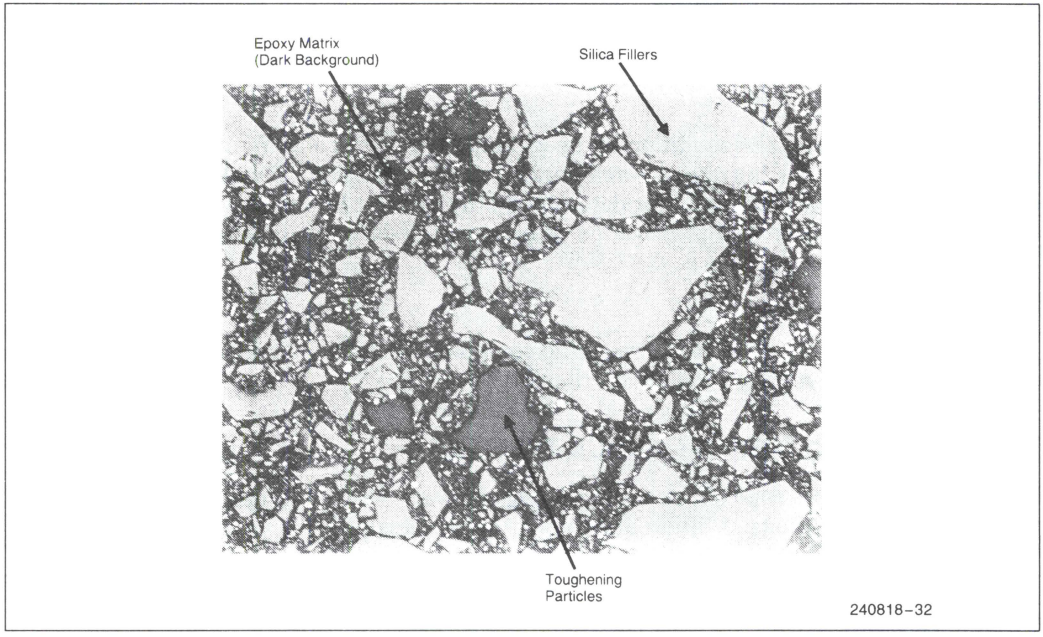


Figure 3-10. Epoxy Molding Compound

Molding Process

Intel suppliers provide partially reacted material in the form of pelletized powder preforms. The epoxy is processed in a transfer molding press, which drives the compound through the heated mold. The viscosity of the molding compound decreases as it comes in contact with the heated mold, allowing it to flow easily around the bonding wires and to fill the package cavity. Viscosity increases as the curing reaction takes place, until the compound is hard enough to be removed from the mold. A schematic plot of molding compound viscosity as a function of time is shown in Figure 3-11, where T_2 is greater than T_1. Figure 3-12 outlines the primary steps in the transfer molding process.

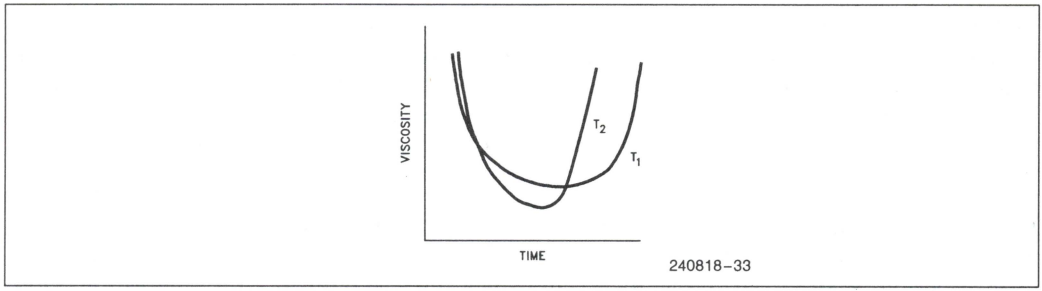


Figure 3-11. Molding Compound Viscosity—Time Behavior (Schematic)

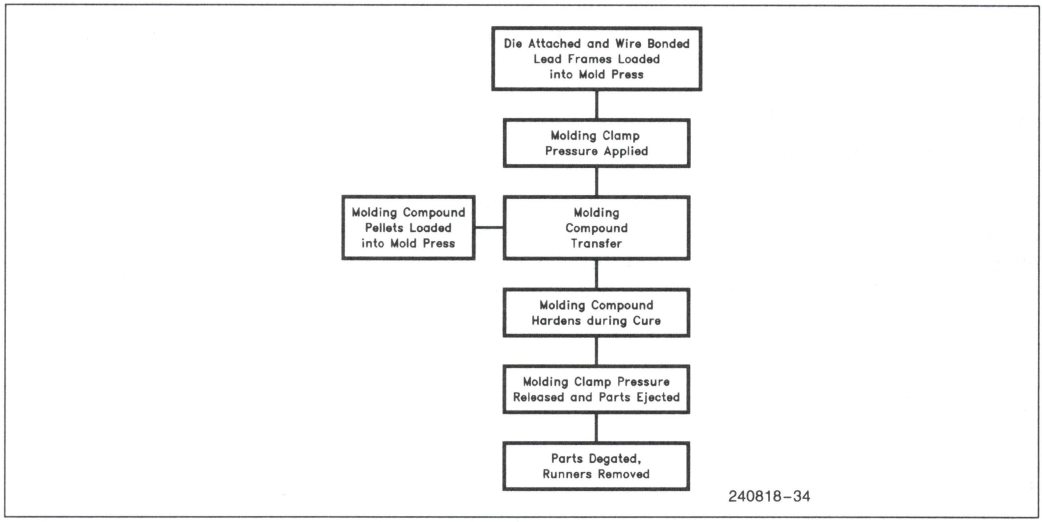


Figure 3-12. Encapsulation Process Flow

Molding process parameters such as cure temperature, compound transfer rate, and cure time are controlled to ensure quality and reliability in the molded part. Of equal importance are the designs of the mold runner and gate systems, the path through which the molding compound enters the package cavity. Intel uses design of experiments (DOE) methodologies that include these variables throughout the development and optimization of the molding process.

Performance/Engineering Considerations

The molded plastic package is a composite system made up of the following:

- A copper alloy or Alloy 42 lead frame
- Silver-filled polymeric die attach adhesive
- Silicon chip
- Gold bonding wires
- Epoxy molding compound

Each of these components has a unique set of physical properties, and mismatches such as those in the coefficient of thermal expansion present a challenge to maintaining the mechanical integrity of the bulk materials and the interfaces between them.

Because of different rates of expansion and contraction, stresses concentrate at the interfaces between materials during the temperature excursions typical of accelerated reliability testing and circuit board mounting. When these stresses exceed the interfacial strength between materials, loss of adhesion can occur. The presence of absorbed moisture in the molding compound exacerbates this phenomenon. The following approaches are taken to prevent failure of the encapsulant during processing, testing, and end use.

From the material perspective, the supplier of the molding compound synthesizes the polymer to exhibit minimum moisture absorption. In addition, coupling agents are used to maximize adhesion between the epoxy matrix and silica filler to limit moisture ingression. Optimization of other material properties, such as flexural strength, modulus, and toughness, ensures that the material can perform under severe moisture and temperature-cycling conditions without the occurrence of cracking, which can lead to the ingress of corrosion-causing contaminants. The molding compound contains elastomeric toughening agents that curtail the growth of cracks should they begin. These "low-stress" materials also provide protection to the fragile chip surface by preventing cracking and shear deformation of the thin-film structures that make up the circuitry.

Careful package and process designs also ensure integrity of the molded package. Package engineers employ design features that provide robustness to the component by creating mechanical locks between molding compound and lead frame. Assembly process engineers design material flows that maximize adhesion and limit exposure to moisture during the manufacture, shipping, and board mounting of the component.

LEAD FINISH

Intel provides four basic lead finishes:

- Gold Plate
- Tin Plate
- SolderCoat
- SolderPlate

Each type of lead finish offers advantages for specific applications and for internal processing.

Gold Plate

The gold-plated finish is recommended for socket applications only. The packages most often involved are the ceramic laminate family, including pin grid arrays (PGAs), side-braze dual in-line packages (DIPs), and both leaded and leadless chip carriers.

Not long ago, gold was considered a universally superior lead finish because of its solderability, and electrical and nonoxidizing properties. During the past several years, however, it has been determined that soldering gold-plated component leads directly into a PC board has clear disadvantages. Excess gold in the solder joints can result in the formation of a brittle alloy, causing the joints to fail over time in high-vibration or board-flexing environments.

For example, in military applications requiring leadless chip carrier mounting, such considerations become critical. Currently, military requirements demand that a solder coat replace gold in direct soldering uses for both leadless and leaded components. Gold plating remains the lead finish of choice for socketed units.

Tin Plate

Intel uses tin plating for selected ceramic DIP (CERDIP) packages only. The tin-plated finish can be either directly soldered or socketed with a non-gold socket contact finish.

Tin offers the advantage of a slightly higher melting point (232°C) than solder (180°C), and it can be burned in at higher temperatures without melting. However, when compared to solder coating, tin plating does not age as well in long-term storage from the standpoint of solderability. This may occur because tin plating is more porous than solder coating. In general, pure tin plating is more susceptible to tin whisker growth under certain mechanical and environmental conditions.

SolderCoat

SolderCoat component leads offers the distinct advantages of a low melting point (180°C) and resistance to aging.

The composition of SolderCoat is the eutectic alloy of 63% tin and 37% lead. Intel normally applies the coating in the following sequence: (1) cleaning the leads, (2) applying a flux, (3) dipping the leads into molten solder, and (4) finishing with a hot water rinse. Great care is taken to minimize any thermal shock to the package and die during SolderCoat processing and cleaning of the unit after coating.

Intel provides SolderCoat lead finish on all plastic and ceramic DIPs, all military packages, and some selected plastic leaded chip carriers (PLCCs). The customer can use this lead finish in a variety of PC board assembly processes, including wave soldering, infrared, and vapor phase.

SolderPlate

Intel uses tin-lead alloy plating for plastic quad fine-pitch, quad flatpack, and PLCC packages.

The codeposited elements form an alloy composition of approximately 85% tin and 15% lead. As shown in Figure 3-13, the plating on the packages' copper lead frames, with a thickness of 200 microinches minimum, provides full coverage of the copper without exposing any formed intermetallics to the air. At the same time, SolderPlate produces a very solderable finish with a melting point of approximately 215°C. Like tin-plated leads, those plated with tin-lead alloy can be directly soldered using infrared or vapor phase methods, or socketed.

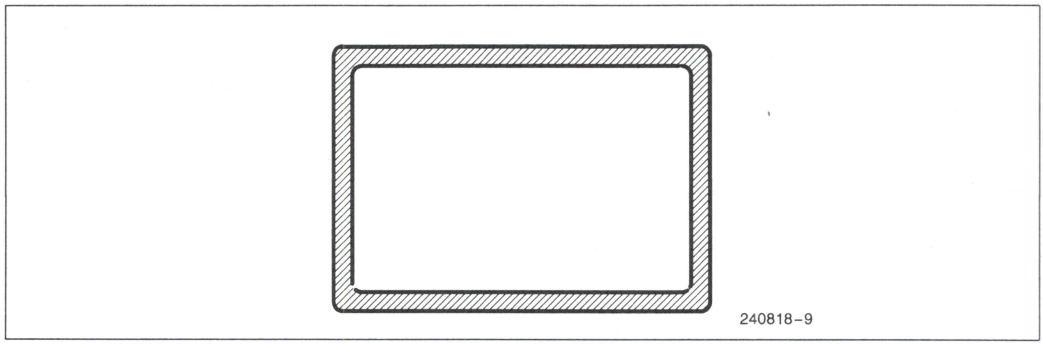


Figure 3-13. Tin or SolderPlating on a Lead Frame

Lead Finish Process Flow

The following sections illustrate the process flow for each type of Intel lead finish.

GOLD

Packages with this finish are purchased from the package vendor as raw piece parts.

SOLDERPLATE

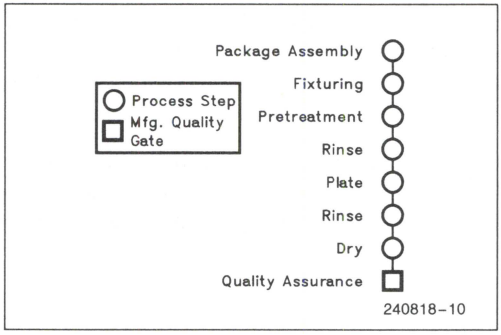


Figure 3-14. Process Flow for Tin and SolderPlating

SOLDERCOAT

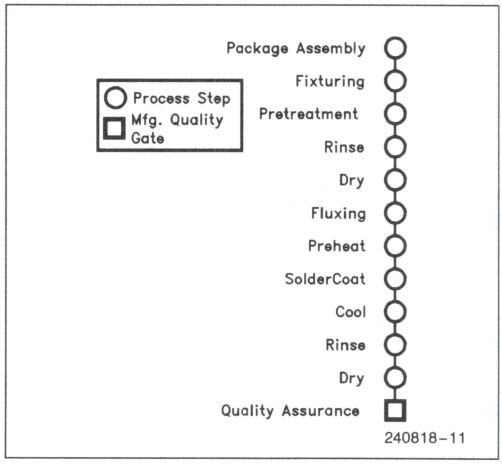


Figure 3-15. Process Flow for SolderCoat

Process Controls

Plating operations are controlled by monitoring a combination of several items:

- Physical arrangement and condition of the plating anodes and fixtures, as well as distance to the work to be plated

- Chemical analysis of plating and pretreatment solutions for all constituents and contaminants, including by-products
- Plating parameters such as temperatures, rinse flows, voltage and current density, and process times

SolderCoat operations are controlled and monitored for many of the same items as plating:

- Physical height of the solder and condition of fixtures
- Chemical analysis of the pretreatment solution and solder
- Operational parameters such as conveyor speed, flux density, preheat temperature, solder temperature, thermal package profiles, and rinse flows and temperatures

Product Controls

In addition to process controls, Intel continues to monitor IC lead-finish functionality using a series of product tests.

Lead-finish thickness and solderability monitors are performed on all products. Intel has also developed a supplementary solderability test to track long-term trends. Alloy thickness and composition are tested in the tin-lead plating operations on a real-time basis. Selected products are also tested for wetting speed.

LEAD FORMING

Lead forming is a twofold assembly operation that bends and trims plated or solder-dipped leads to meet specified dimensional accuracy. Leads can be formed into three standard configurations: gull-wing and J-lead for surface mount packages, and straight form for through-hole mounting. During the forming process, extreme care is taken to expose the tin-plated or solder-coated leads to minimum stress and abrasion, thus ensuring maximum strength and reliability.

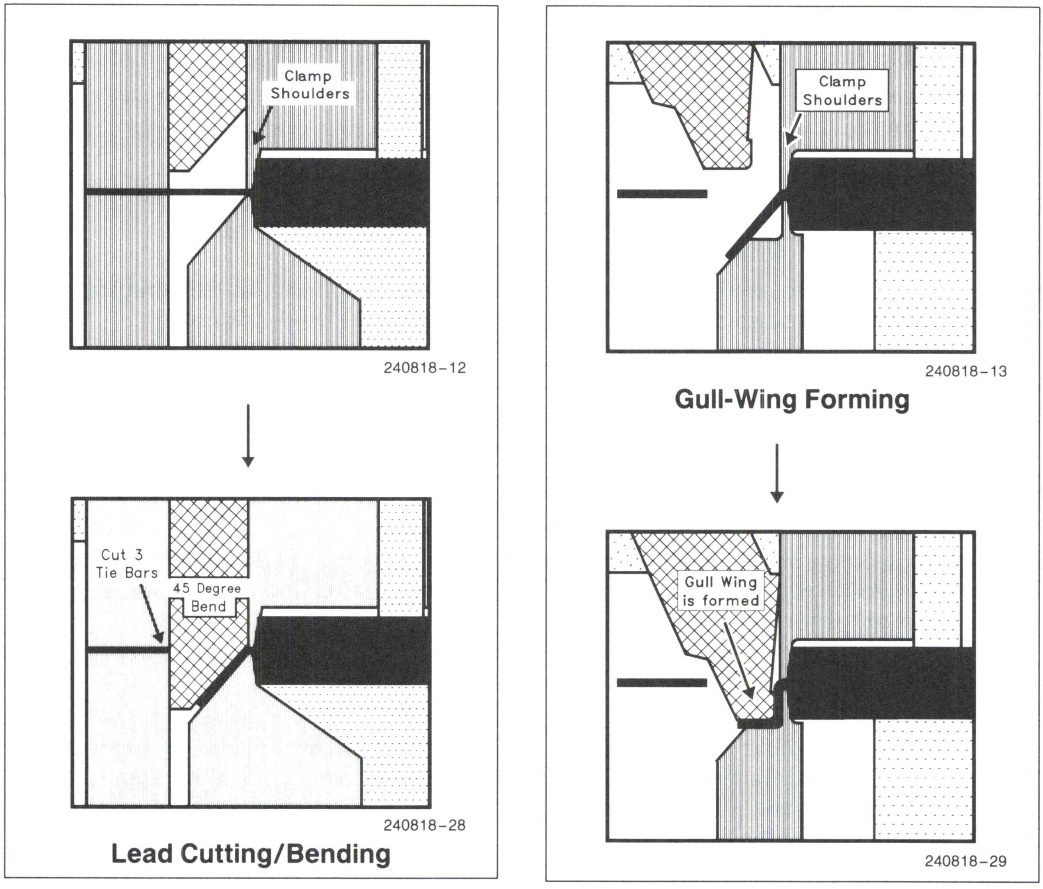


Figure 3-16. Formation of Gull-Wing Leads

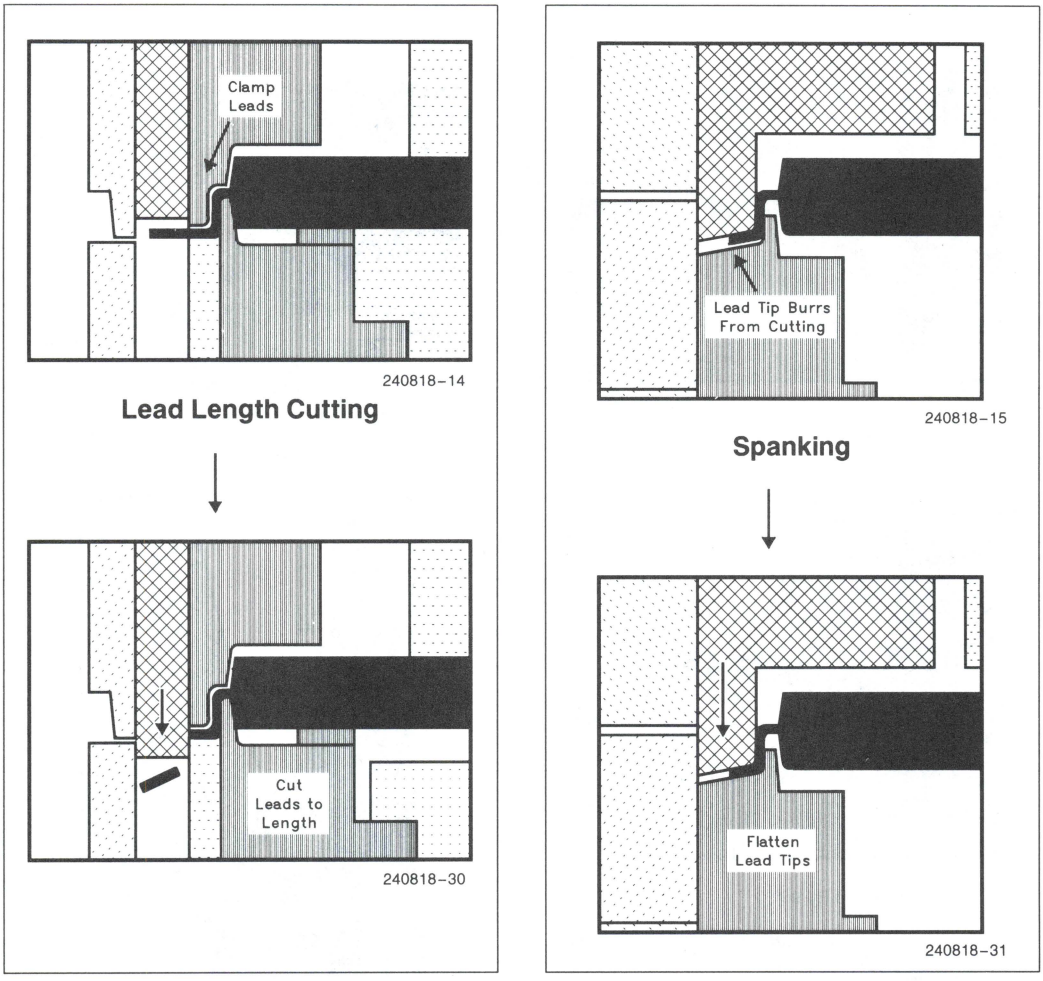
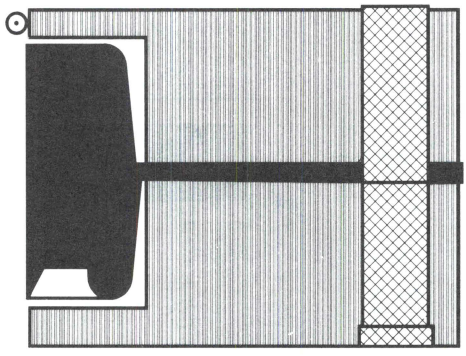
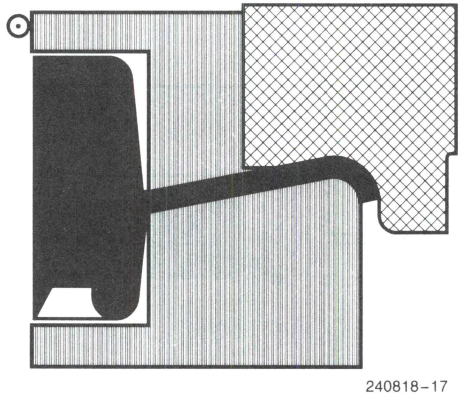


Figure 3-17. Formation of Gull-Wing Leads (Continued)



240818-16

Step 1. Lead Length Cut



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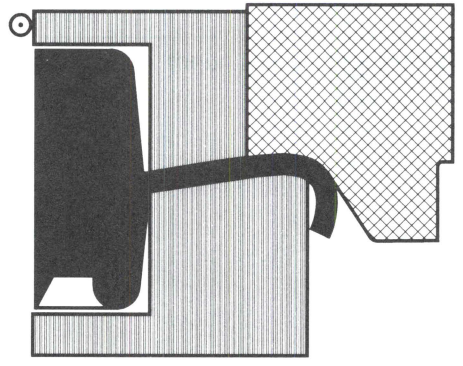
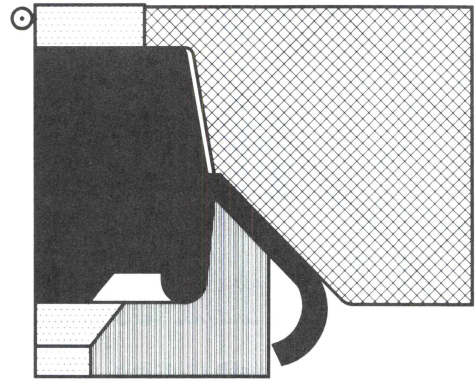
Step 2. Lead Tip Bend By 90°



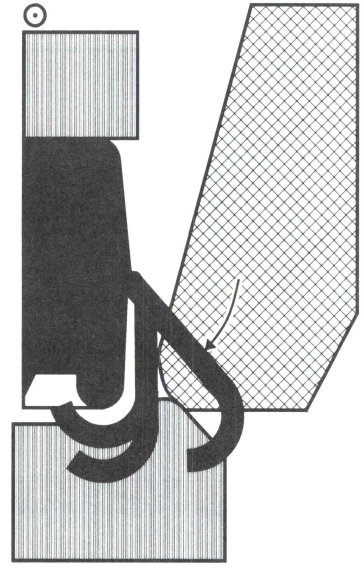
240818-18

Step 3. More Lead tip Bend. Total of 140°



240818-19

Step 4. Shoulder Bend by 45°



240818-20

Step 5. Shoulder Bend by 90° and Final Curl by Calibration Block

Figure 3-18. Deflash, Trim, and Form of J-Leads on PLCCs

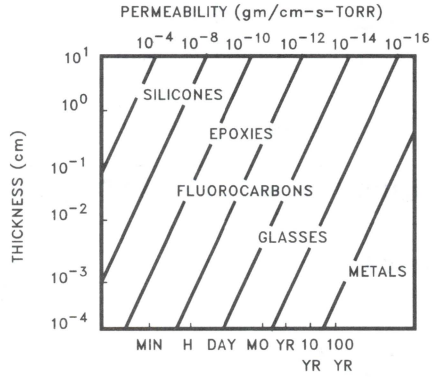
As part of the lead-forming process, dambars and excess molding compound or flash that has flowed between the leads and out to the dambars are removed simultaneously from the leads. This step electrically isolates the leads.

Finally, individual units are separated or singulated from the lead frame at the tie bar support and carefully placed into tubes or trays for lead protection. Singulation is either combined with the forming operation or occurs separately after forming.

HERMETIC SEALING

Packaging Options

Hermetic sealing of IC packages is used to seal the silicon electronic component from the external environment, specifically from water vapor and contaminants that can shorten the lifetime of a sensitive electronic device. Two types of hermetic seals are used at Intel: hard-solder precious metal brazing alloys (the laminated ceramic package family) and low melting-temperature glasses (the pressed ceramic package family). The metal-sealed packages are of the laminated ceramic type and involve the brazing of a metal lid to a gold-plated thick-film seal ring on the ceramic. The glass-sealed packages utilize glass to create the seal between pressed ceramic pieceparts. Figure 3-19 illustrates the relative hermeticity of various sealing materials. It can be seen from the graph that metal seals provide the highest levels of hermeticity, followed by glasses and ceramics.



Time required to achieve 50% of exterior humidity for various sealant materials

Figure 3-19. Relative Hermeticity of Materials

Materials

METAL-SEALED LAMINATED CERAMIC PACKAGES (CX PACKAGES)

Of the two hermetic package families, metal-sealed packages provide higher levels of hermeticity and reliability. At Intel, the metal-sealed packages utilize a gold-tin eutectic hard solder to create the hermetic seal. The composition of the alloy is 80% gold, 20% tin, and has a

melting point of 280°C (see Figure 3-20). This solder was chosen for its excellent wetting characteristics to the seal ring and lid materials, as well as its high resistance to thermal fatigue. Seals created by the Au-Sn alloy can withstand thousands of condition C thermal cycles without failure.

The gold-tin eutectic seal is made to a seal ring on the surface of the aluminum oxide ceramic. The seal ring is composed of a tungsten thick film that is fired to the ceramic material and plated with a thin nickel diffusion barrier and a gold overplate. The gold overplate prevents oxidation and provides a wettable surface for the solder. Figure 3-21 is a schematic of the seal area.

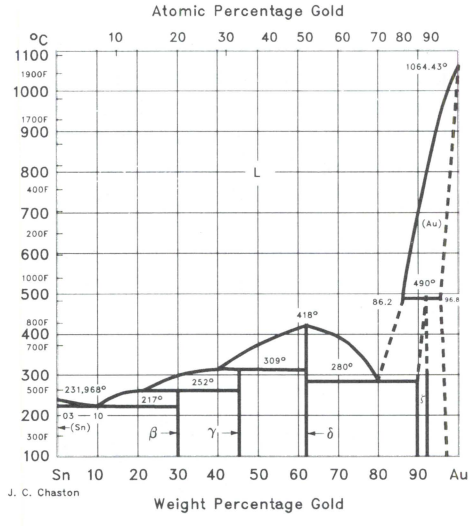


Figure 3-20. Au-Sn Phase Diagram

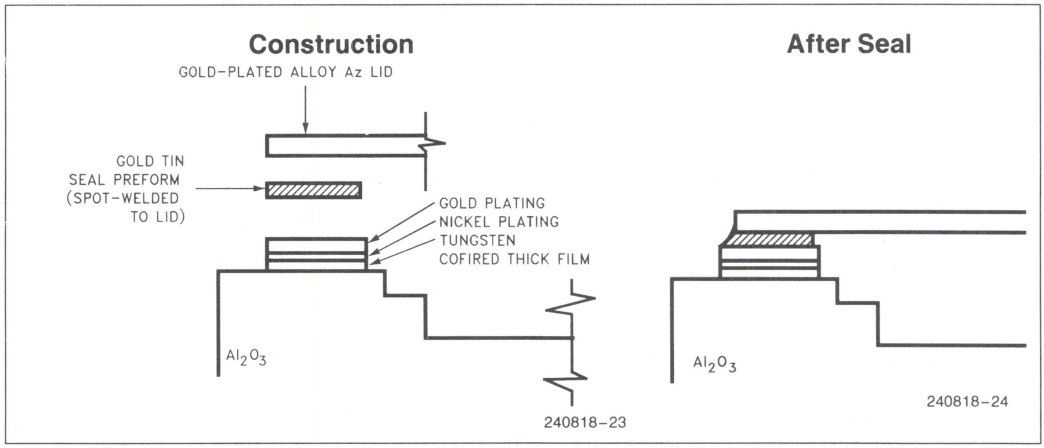


Figure 3-21. Schematic Cross-Section of a CX Package Seal (Thicknesses Not To Scale)

The lid material is gold-plated Alloy 42 (a nickel-iron alloy with low thermal expansion) to which is attached an 80% gold, 20% tin alloy (eutectic composition) preform. The seal preform is attached by spot welding. The lid material was chosen for its stiffness and because the thermal expansion of Alloy 42 is close to that of aluminum oxide ceramic. The stiffness prevents damage during testing, and the low thermal expansion minimizes stress at the seal due to thermal expansion mismatch.

The thicknesses of the plating used in the seal ring area are important to the success of sealing using this system. The thickness of the gold must be controlled to prevent premature nickel diffusion and oxidation at the gold surface, which can create a poorly wetted surface that will result in seal defects. The nickel diffusion barrier prevents the interdiffusion of tungsten and gold that can also result in seal defects.

The seal preform width and thicknesses are also specified to ensure that an adequate amount of solder is present to create a continuous seal. Too large a preform can result in excess solder that can bleed onto the lid surface.

GLASS-SEALED PRESSED CERAMIC PACKAGES

In glass-sealed packages, a ceramic lid is sealed to the base ceramic with a vitreous (noncrystallizing), lead-based glass having a low melting temperature. The glasses chosen for hermetic sealing are lead-zinc borates that generally seal in the 415-450°C range. Figure 3-22 illustrates the vitreous glass-forming region (region A) in the lead-zinc-borate system from which these glasses are chosen. The glasses used in the industry have compositions in this range, with the final selection based on obtaining the lowest possible processing temperature. As a result, the most commonly available seal glasses have very similar compositions. The glasses are highly resistant to chemical plating baths (see Table 3-5) and have excellent thermal shock resistance.

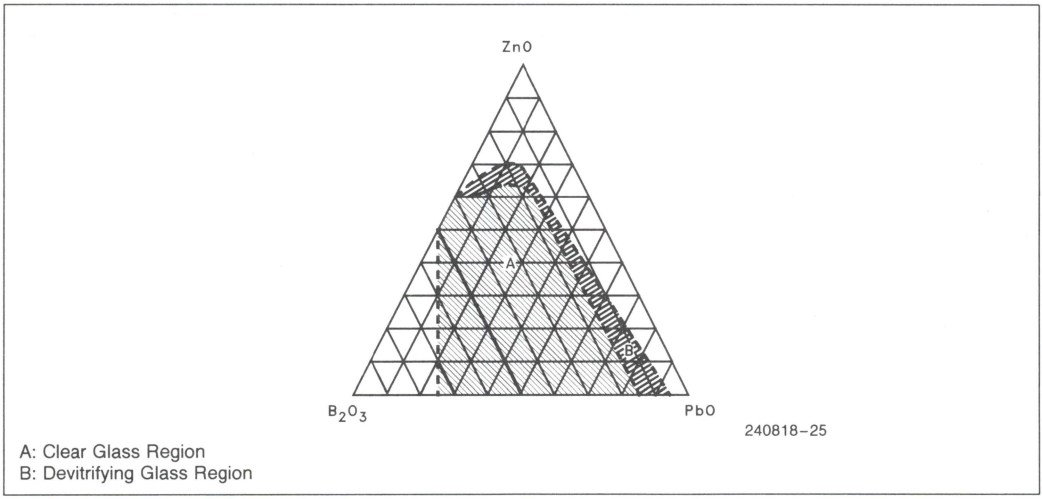


Figure 3-22. Lead-Zinc-Borate Phase Diagram

Table 3-5. Chemical Durability of Glasses Weight Loss ($mg/cm^2/hr$)

Chemical Treatment	Glass Type			
	Intel	B	C	D
50% H_2SO_4, 95°C, 1 hr.	8.65	2.32	5.89	0.88
50% H_2SO_4, 25% HNO_3, 25°C	28.44	25.44	25.32	18.00
5% HNO_3, 25°C, Direct Transfer to 50% H_2SO_4 at 95°C	323.60	385.60	226.80	250.80

*Glasses must exhibit chemical durability in order to withstand the lead-plating baths.

The glasses used for package sealing have high thermal expansions relative to the ceramic. To reduce thermally induced package stresses, it is necessary to reduce the thermal expansion of the glasses by adding low-thermal-expansion fillers. These fillers are chosen to be compatible with the lead glass and do not react during processing.

Because the glasses all have similar compositions, they have similar strengths. Table 3-6 lists the measured bending strengths for several different sealing glasses commonly used. The glass used by Intel can be seen to have bending strengths equivalent to other commonly used glasses. The fracture toughness of Intel's sealing glass is also found to be quite similar. It is expected that the mechanical performance of Intel's sealing glass will be equivalent to other commonly used glasses.

Table 3-6. Bending Strengths and Fracture Toughnesses of Several Lead-Based Sealing Glasses

Glass	Four Point Bending Strength (MPa)	Fracture Toughness ($MPa\sqrt{m}$)
Intel	20.1	1.0
B	21.4	1.1
C	20.0	0.9

Figure 3-23 is a schematic cross-section of a glass-sealed package.

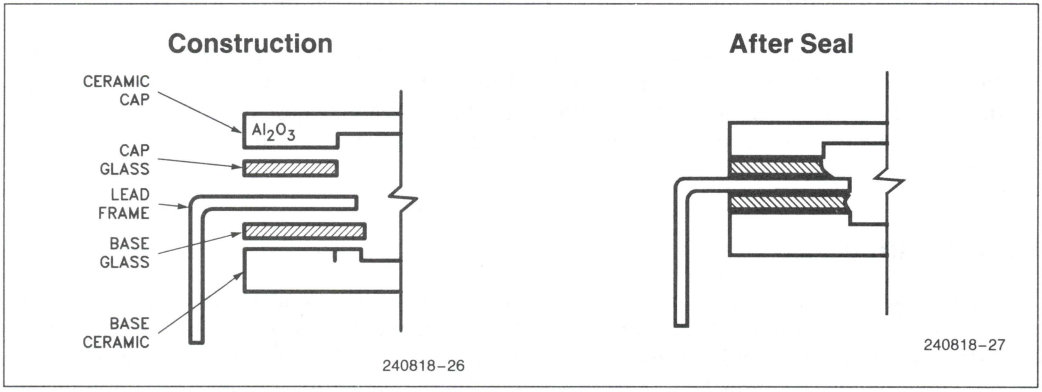


Figure 3-23. Cross Section of a Glass-Sealed Package

Processes

LAMINATED CERAMIC PROCESSING

Sealing of metal-sealed packages is accomplished in a continuous belt furnace. The metal lid is centered and clipped in place to ensure that the seal ring and preform remain properly aligned and that sufficient pressure is exerted on the lid to provide good contact. The units are ramped in temperature past the melting temperature of the alloy and allowed to soak at the sealing temperature. The soak period allows the molten metal time to wet all the sealing surfaces sufficiently and to form an integral metallurgical bond with the seal ring and lid plating.

Sealing can be accomplished in either an inert (nitrogen) or reducing atmosphere (forming gas N_2H_2). The seals obtained with either atmosphere are equivalent in performance. The reducing atmosphere is used to build additional margin into the sealing process.

The sealing process is controlled by monitoring the seal temperatures with a thermocouple embedded in a package that is passed through a fully loaded furnace. This ensures that the furnace profile obtained is representative of that seen by actual product. Water vapor content of the sealing atmosphere is also controlled to ensure that the final internal-cavity water vapor levels meet industry requirements.

PRESSED CERAMIC PROCESSING

Glass-sealed packages are sealed in a continuous dry air atmosphere belt furnace. Caps and bases are held in fixtures during the seal process to provide proper alignment of the top and bottom of the package. No clips are used; the weight of the package is sufficient to create the seal. Because glass does not have a sharp melting point, it is necessary to hold the units at the seal temperature for sufficient time to allow the glass to flow and wet the metal lead frame and ceramic, thus creating the final seal. Insufficient time will result in noncontinuous seals or incomplete flow, causing glass depressions between the leads. These depressions in their worst form can create a continuous path to the cavity (nonhermeticity), or in less severe

cases act as a stress riser and result in package damage during subsequent handling. Sealing is performed in an oxidizing ambient (dry air) to prevent reduction of the lead glass.

As with the metal-sealed packages, the process is controlled by profiling a fully loaded furnace by means of a thermocouple embedded in a CERDIP-type package, again to get an accurate representation of the actual sealing conditions. Water vapor content and flow rates of the atmosphere are controlled to ensure that the internal-cavity water vapor requirements are met.

Performance

Intel's hermetic packages are tested individually for hermeticity using two tests: fine and gross leak. Two tests are required, since neither test can adequately detect the entire range of leak sizes. Fine leak uses helium and a mass spectrograph to identify fine leaks. Larger leaks do not show up, as the gases leak out too quickly for the detectors to identify. The industry-acceptable leak rate for hermetic packages is less than 5×10^{-8} Std. CC atm/min.

Gross leak testing, which identifies larger leaks that fine leak cannot detect, employs a high-vapor pressure fluorocarbon liquid as the detection medium. The unit is pressurized in a container of the fluorocarbon to force the liquid into potential leakage paths. After pressurization, the unit is immersed in a hot bath, which vaporizes the fluorocarbon trapped in the leak. A steady stream of bubbles indicates the location of the leak. The gross leak test cannot be used for small leaks, as the liquid will not penetrate leaks smaller than a certain size.

REVISION SUMMARY

- Added Cyanate Ester references
- Replace Kovar with Alloy 42

Performance Characteristics of IC Packages

4

CHAPTER 4
PERFORMANCE CHARACTERISTICS OF IC PACKAGES

IC PACKAGE ELECTRICAL CHARACTERISTICS

The following parameters are provided for Intel packages:

- DC resistance (R) of leads or pins
- Capacitance (C), including lead-to-lead and loading capacitances
- Inductance (L), including only self-inductance values for pins, traces and wires (PGA) or leads and wires (plastic).

These parameters can be experimentally measured and theoretically calculated. The package parameters for the following package families are representative of measured, or calculated, values:

- Plastic quad flatpack (PQFP)
- Multilayer molded package (MM-PQFP)
- Ceramic quad flatpack (CQFP)
- Pin grid array (PGA)
- Plastic leaded chip carrier (PLCC)
- Quad Flatpack (QFP, SQFP, TQFP)

The MM, CQFP, and PGA packages can be designed with ground and power planes. Since these packages are custom-designed for each product, their parameters may not reflect the actual values for a particular product. The actual parameters can be obtained by contacting Intel.

For electrical parameters of packages not listed in the tables, please contact your local Intel field sales engineer.

Package Electrical Data

Following are the electrical characteristics of Intel's PGA packages. The three parameters discussed are D.C. resistance (R), capacitance (C), and inductance (L). A summary of typical ranges of values is presented in Table 4-1.

Table 4-1. Summary of PGA Electrical Data

Electrical Parameter	Lead Count								
	68 PGA			88 PGA			132 PGA		
	Min	Ave	Max	Min	Ave	Max	Min	Ave	Max
L_{Trace} (nH)	1.1	3.8	6.5	1.4	4.5	7.7	1.1	4.8	8.5
R_{Trace} (Ω)	0.173	0.584	0.994	0.215	0.696	1.178	0.173	0.740	1.307
$L_{Bondwire}$ (nH)	1.5	2.1	2.7	1.5	2.1	2.7	1.5	2.1	2.7
$R_{Bondwire}$ (Ω)	0.045	0.058	0.072	0.045	0.058	0.072	0.045	0.058	0.072
$L_{VCC/VSS\ Trace}$ (nH)	1.0	1.7	2.5	1.0	1.7	2.5	1.0	1.7	2.5
$R_{VCC/VSS\ Trace}$ (Ω)	0.150	0.263	0.375	0.150	0.263	0.375	0.150	0.263	0.375
L_{Pin} (nH)	0.7	1.0	1.4	0.7	1.0	1.4	0.7	1.0	1.4
R_{Pin} (Ω)	0.004	0.005	0.006	0.004	0.005	0.006	0.004	0.005	0.006

Electrical Parameter	Lead Count								
	168 PGA			208 PGA			240 PGA		
	Min	Ave	Max	Min	Ave	Max	Min	Ave	Max
L_{Trace} (nH)	1.4	5.8	10.3	1.4	6.0	10.7	1.4	6.6	11.8
R_{Trace} (Ω)	0.286	1.193	2.100	0.286	1.234	2.183	0.286	1.346	2.405
$L_{Bondwire}$ (nH)	1.5	2.1	2.7	1.5	2.1	2.7	1.5	2.1	2.7
$R_{Bondwire}$ (Ω)	0.045	0.058	0.072	0.045	0.058	0.072	0.045	0.058	0.072
$L_{VCC/VSS\ Trace}$ (nH)	1.0	1.7	2.5	1.0	1.7	2.5	1.0	1.7	2.5
$R_{VCC/VSS\ Trace}$ (Ω)	0.200	0.350	0.500	0.200	0.350	0.500	0.200	0.350	0.500
L_{Pin} (nH)	0.7	1.0	1.4	0.7	1.0	1.4	0.7	1.0	1.4
R_{Pin} (Ω)	0.004	0.005	0.006	0.004	0.005	0.006	0.004	0.005	0.006

Electrical Parameter	Lead Count											
	280 PGA			272 PGA			320 PGA			360 PGA		
	Min	Ave	Max	Min	Ave	Max	Min	Ave	Max	Min	Ave	Max
L_{Trace} (nH)	1.4	6.8	12.2	1.5	7.2	13.0	1.5	7.4	13.4	1.5	7.6	13.8
R_{Trace} (Ω)	0.286	1.388	2.491	0.297	1.471	2.645	0.297	1.512	2.727	0.297	1.556	2.815
$L_{Bondwire}$ (nH)	1.5	2.1	2.7	1.5	2.1	2.7	1.5	2.1	2.7	1.5	2.1	2.7
$R_{Bondwire}$ (Ω)	0.045	0.058	0.072	0.045	0.058	0.072	0.045	0.058	0.072	0.045	0.058	0.072
$L_{VCC/VSS\ Trace}$ (nH)	1.0	1.7	2.5	1.0	1.7	2.5	1.0	1.7	2.5	1.0	1.7	2.5
$R_{VCC/VSS\ Trace}$ (Ω)	0.200	0.350	0.500	0.200	0.350	0.500	0.200	0.350	0.500	0.200	0.350	0.500
L_{Pin} (nH)	0.7	1.0	1.4	0.7	1.0	1.4	0.7	1.0	1.4	0.7	1.0	1.4
R_{Pin} (Ω)	0.004	0.005	0.006	0.004	0.005	0.006	0.004	0.005	0.006	0.004	0.005	0.006

Table 4-2. Summary of CQFP Electrical Data

Electrical Parameter		Lead Count	
		164L	196L
L_{Lead}	nH	3.3	3.3
R_{Lead}	Ω	0.004	0.004
$L_{Trace\ (I/O)}$	nH	5.0	6.0
$R_{Trace\ (I/O)}$	Ω	0.8	0.9
C_{Load}	pF	4.0	5.0
$L_{Trace\ (V_{CC}/V_{SS})}$	nH	1.5	2.5
$R_{Trace\ (V_{CC}/V_{SS})}$	nH	0.2	0.4
L_{Wire}	nH	3.0	3.0
R_{Wire}	Ω	0.08	0.08
$C_{(V_{CC}\ Plane\ to\ V_{SS}\ Plane)}$	pF	170.0	240.0

Table 4-3. Summary of MM Packages

Electrical Parameter	Lead Count			
	132 Lead MM		196 Lead MM	
	Min	Max	Min	Max
I/O				
$R_{Wire\ +\ Lead}$ (mΩ)	81	106	83	115
$L_{Wire\ +\ Lead}$ (nH)	6.6	8.3	7.6	10.2
C_{load} (pF)	0.5	1.3	0.7	2.2
V_{SS} and V_{CC}				
$R_{V_{SS}\ db\ Wire}$ (mΩ)	34	34	34	34
$L_{V_{SS}\ db\ Wire}$ (nH)	1.1	1.1	1.1	1.1
$L_{V_{SS}\ Plane}$ (nH)	0.2	0.2	0.3	0.3
C_{plane} (nF)	0.090	0.090	0.210	0.210
$R_{V_{CC}\ db\ Wire}$ (mΩ)	55	55	55	55
$L_{V_{CC}\ dB\ Wire}$ (nH)	1.9	1.9	1.9	1.9
$L_{V_{CC}\ Plane}$ (nH)	0.2	0.2	0.3	0.3
$R_{lead\ to\ Pin}$ (mΩ)	9	10	10	12
$L_{lead\ to\ Pin}$ (mΩ)	3.8	4.2	4.7	5.3

DEFINITIONS:
db—Down bond

Table 4-4. Summary of PQFP Electrical Data

Electrical Parameter	Lead Count							
	84 Lead PQFP		100 Lead PQFP		132 Lead PQFP		164 Lead PQFP	
	Min	Max	Min	Max	Min	Max	Min	Max
$R_{Wire + Lead}$ (mΩ)	62.9	106.4	64.9	108.8	63.2	112.8	65.8	116.9
$L_{Wire + Lead}$ (nH)	5.3	9.8	5.9	10.6	5.4	11.9	6.2	13.2
C_{load} (pF)	0.2	0.6	0.3	0.7	0.2	0.9	0.3	1.0

Table 4-5. Summary of PLCC Electrical Data

Electrical Parameter	Lead Count							
	28 Lead PLCC		32 Lead PLCC		44 Lead PLCC		68 Lead PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max
$R_{Wire + Lead}$ (mΩ)	56.7	74.0	56.9	74.3	57.7	75.6	57.7	78.4
$L_{Wire + Lead}$ (nH)	4.1	7.1	4.2	7.3	5.0	8.4	5.0	10.3
C_{load} (pF)	0.2	0.6	0.2	0.7	0.3	0.8	0.3	1.2

Table 4-6. Summary of QFP Electrical Data

Electrical Parameter	Lead Count					
	44 Lead QFP		64 Lead QFP		80 Lead QFP	
	Min	Max	Min	Max	Min	Max
$R_{Wire + Lead}$ (mΩ)	60.9	102.3	60.9	102.0	61.8	108.6
$L_{Wire + Lead}$ (nH)	4.8	8.7	4.8	8.6	5.1	10.8
C_{load} (pF)	0.1	0.4	0.1	0.4	0.1	0.6

Table 4-7. Summary of SQFP/TQFP Electrical Data

Summary	Lead Count									
	80 Lead SQFP		100 Lead SQFP		144 Lead TQFP		176 Lead TQFP		208 Lead SQFP	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
$R_{Wire + Lead}$ (mΩ)	61.5	82.6	61.8	84.6	69.5	98.1	69.5	103.7	69.5	122.6
$L_{Wire + Lead}$ (nH)	4.0	6.4	4.1	6.9	5.2	8.7	5.2	9.8	6.3	12.6
C_{load} (pF)	0.2	0.4	0.2	0.5	0.3	0.7	0.3	0.8	0.4	1.0

Electrical Parameters

DC RESISTANCE (R)

The DC resistance is normally the cause of IR voltage drops. Reduction of DC resistance is particularly important in the ground and power paths. The relatively high resistance of the traces in the ceramic package is due to material and geometry (thickness, 0.001 in.; width, 0.006 in.; and various lengths). The resistance per square centimeter of tungsten used is 0.010Ω.

CAPACITANCE (C)

Capacitance is determined by the (1) length of the leads, (2) distance separating the leads, (3) dielectric constant of the material between them, (4) lead thickness, and (5) number of leads involved. Larger leads have larger values of capacitance. The relative dielectric constant of the material used for ceramic PGAs is in the range of 8-10. The dielectric constant for plastic package material is around 4-6.

Capacitance is classified as "loading" or "lead-to-lead". The loading value represents the capacitance of a single lead in the presence of a system of conductors. It is greater than the lead-to-lead value, which represents the capacitance between two leads with all other conductors grounded. The loading capacitances are the diagonal terms in the C matrix, and lead-to-lead capacitances are the off-diagonal terms.

INDUCTANCE (L)

The inductance value is influenced by the package size and the location of the leads in a given circuit with respect to the power and ground locations. The inductance of the I/O lines is due to the circuit loop created by the current-in and current-out paths. If the loop area is smaller, effective inductance is also smaller. Shorter, wider leads have smaller values of inductance. For multiple switching, the concept of a loop breaks down and must be replaced with the inductance matrix, which consists of self-inductance and mutual inductance. For multilayer packages with power and ground planes, the problem is not severe, because the mutual inductance (off-diagonal) terms in the matrix are small compared to the self-inductance (diagonal) terms.

THEORETICAL CALCULATIONS

The theoretical values for package parameters are obtained by using an Intel proprietary software package called iPEST (Intel Package Electrical Simulation Tool). This software calculates the inductance, capacitance, and resistance values from the CAD-based geometry information and material properties.

For single-layer packages without power and ground planes, the complete inductance matrix for the leads can be calculated. The software computes the parameters for each component of the package, such as trace, lead, bond wire and pin.

Measurement Methods

RESISTANCE

The resistance for a given package is measured from the tip of the bond finger to the pin braze pad. The lead resistance for plastic packages is measured from tip to tip.

Figure 4-1 shows the four-probe set-up used to measure the resistance values. Two sets of readings are taken by reversing the direction of current to eliminate the contact potential. The average value is considered the resistance of the sample.

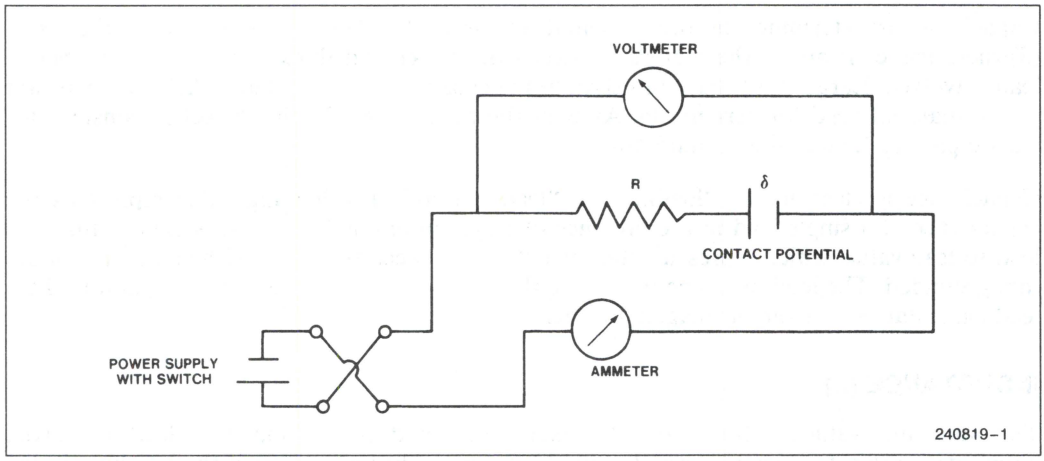


Figure 4-1

CAPACITANCE

Capacitance measurements are made using two separate methods. The first method measures the capacitance of a single lead in the presence of a system of conductors (loading capacitance). In this method, all leads except one are grounded and then the capacitance of the remaining lead is measured with respect to ground, as shown in Figure 4-2.

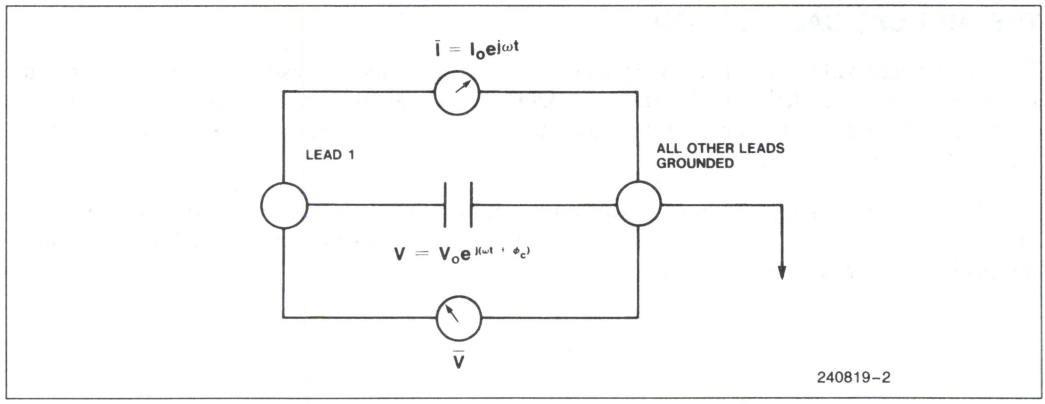


Figure 4-2

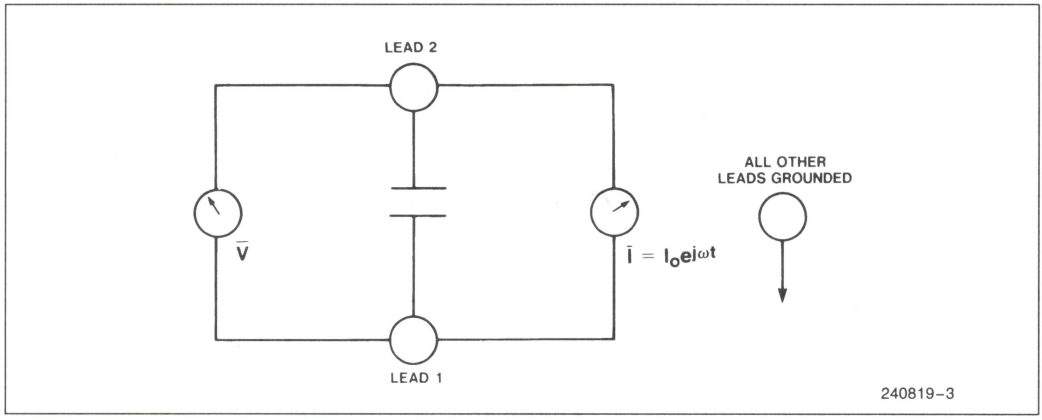


Figure 4-3

The measurements are performed using a current source having frequency f and then by measuring the voltage drop and phase shift across the sample. For pure capacitance, the phase shift is $(-\pi/2)$.

INDUCTANCE

As shown in Figures 4-4 and 4-5, the inductance is measured in a circuit that includes internal wires bonded from each of two arbitrarily chosen leads to a metal plate on the die pad (in place of a silicon chip).

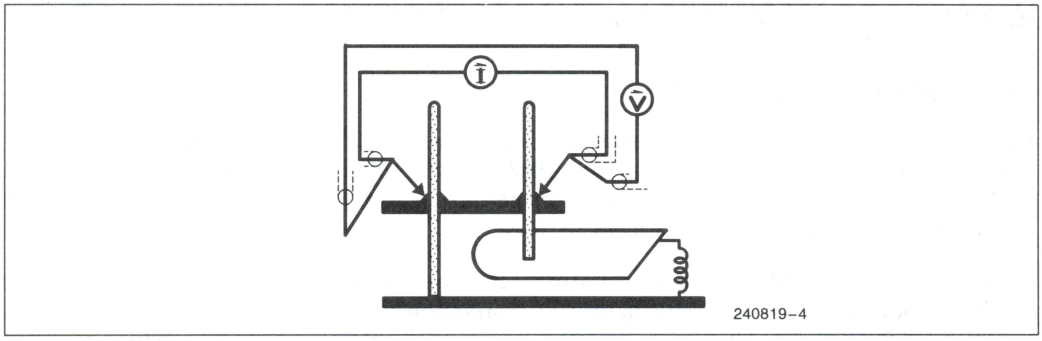


Figure 4-4

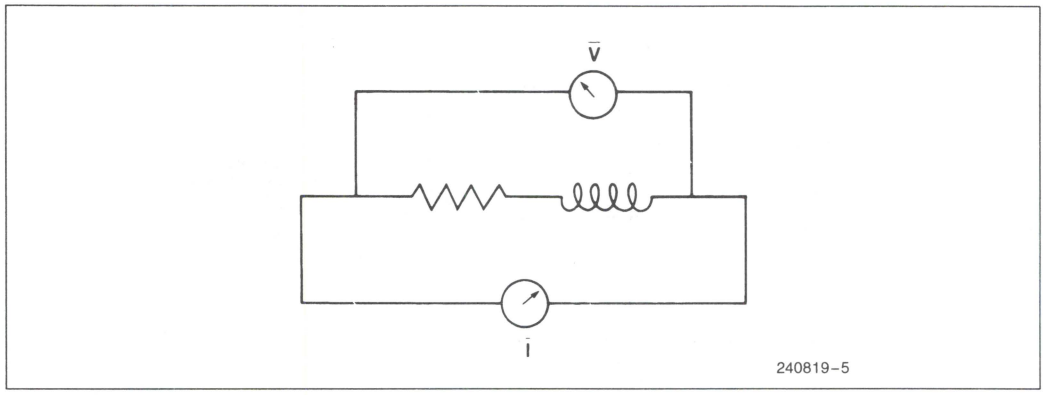


Figure 4-5

For I/O lines, the current enters the trace and is distributed in the ground plane. The interaction of the current in the trace with the current distributed in the ground plane determines the effective inductance. In PGA packages, the magnetic field is primarily contained in a plane perpendicular to the X-Y plane containing the I/O trace. This helps to keep the mutual coupling between two traces to a minimum.

Like capacitance measurements, inductance measurements use a current source having frequency f. By measuring the voltage drop and the phase shift across the sample, one can determine the inductance. For a pure inductive circuit, the phase shift is $(+\pi/2)$.

IC PACKAGE MECHANICAL CHARACTERISTICS

Sources of Stress

Each assembly step is a potential stress-inducing operation: Silicon chipping and metal peeling can occur during the saw process; die backside damage and chipping during the die attach process; bond pad and silicon substrate damage during wire bonding; and wire bond sweep during encapsulation (plastic packages).

In addition, accelerated environmental stress tests can introduce failure modes that require detailed modeling to provide satisfactory interpretation of the results and extrapolation to failure rates in the field. These accelerated tests include thermal cycling to produce repeated thermal stresses, and shock and vibration to produce dynamic and oscillatory mechanical loads on the package and its contents.

The ability of the package to withstand these stress-inducing environments is governed by the properties of the materials used in construction, as well as by the design geometry. The key material properties are (1) elastic modulus, (2) density, and (3) linear coefficient of thermal expansion (CTE). The modulus is required in all models, while density is needed in dynamic analyses, and CTE is needed in thermal analyses. These properties are listed in Table 4-8 for key packaging materials. Commonly referenced geometric design variables include length (L) and thickness (h) of elements making up layers in the packages.

Table 4-8. Room Temperature Material Properties

Material	Elastic Modulus (GPa)	Density (kg/ltr)	Coefficient of Thermal Expansion $(MC)^{-1}$
Silicon	150	2.3	4.2
Die Attach	5*	2.9	50.0*
Aluminum	70	2.7	23.0
Copper	120	9.0	17.0
Gold	80	18.9	14.3
Alloy 42	145	7.8	6.4
Molding Compound	14.2	1.80	17.0*
Al_2O_3	265	3.99	5.0
Solder	8.3	9.3	26.0

NOTE:
*Below T_g, glass transition temperature (~100°C, die attach adhesive; −175°C, molding compound)

Stress, Strength, and Beyond

Much of Intel's stress-modeling word performed using 2-D or 3-D finite element analysis (FEA) methods is based on elastic material behavior. The limit to this behavior is governed by the type of material being analyzed. For brittle materials such as silicon, ceramics, and molding compounds, fracture initiation represents the limit to the elastic model. For ductile materials such as aluminum, copper, gold, Alloy 42, and solder, onset of plastic flow becomes the limit.

While the same 2-D/3-D stress analysis applies to both brittle and ductile materials up to their elastic limits, different stress parameters must be calculated to determine if the elastic limit has been reached. For brittle materials, the maximum principal stress, which is proportional to the sum of the normal stresses, is compared to the ultimate tensile strength. Alternatively, the stress intensity (again principal stress driven) may be compared to the fracture toughness. For ductile materials, the effective stress, which is a measure of the maximum shear stress, is compared to the yield strength. Representative fracture toughnesses (K_{IC}), ultimate tensile strengths (σ_u), and yield strengths (σ_y) are listed in Table 4-9. Because interfacial adhesion strengths also govern the onset of delamination, these are listed under σ_u in the table for bimaterial interfaces of interest.

Table 4-9. Fracture Toughness and Ultimate and Yield Strengths for Selected Materials (Room Temperature Data)

Material	K_{IC} (MPa $m^{1/2}$)	σ_u (MPa)	σ_y (MPa)
Silicon	0.8	150	
Ceramic		300	
Molding Compound	2.0	100	
Aluminum (Annealed)			20
Copper Alloy			415
Gold			165
Alloy 42			275
Solder			25
Si/MC		14	
Cu/MC		7	
Al/PI	0.02		

Beyond the elastic limit, the linear stress-strain relationships must be supplemented with crack growth formulas for brittle materials and with plastic flow rules for ductile materials. The resulting constitutive equations are nonlinear and computation-intensive. They provide a mathematical description of irreversible processes that can lead to functional failures in the product if sufficient cyclic operations are completed. When supplemented with experimental data, these post-elastic solutions are useful in providing product life estimates (reliability prediction).

Applications

BASIC ANALYSIS

To determine thermally and mechanically induced package stresses, Intel uses both modeling and measurement methods. Modeling is carried out at three levels: (1) laminated beam analyses to establish trends as design and material properties are varied; (2) 2-D FEA when the limits of the strength of materials model are reached for configurations that can be modeled as plane stress or strain; and (3) 3-D FEA for configurations that defy simplification.

Measurement of stresses on the device surface is performed with piezoresistive elements (pressure-sensitive resistors) diffused onto the surface of the silicon device. Under stress (strain), the resistance of the elements changes and can be detected using simple bridge circuits. Comparison of predictions and measurements provides an important self-check on the two modeling tools used for stress analysis.

Intel uses ANSYS software, a trademark of Swanson Systems Inc., for the 2-D and 3-D FEA modeling. Because it allows for nonlinear material behavior (elastic, plastic, and creep), it is a powerful analytical tool. In addition, it is widely accepted in the electronics industry and has become a de facto standard.

RESIDUAL THERMAL STRESSES IN PLASTIC PACKAGES

Die-level stresses are created during die attach for ceramic and plastic packages, and during encapsulation for plastic packages. Representative stresses are shown in Figure 4-6 for die attach and in Figure 4-7 for encapsulation.

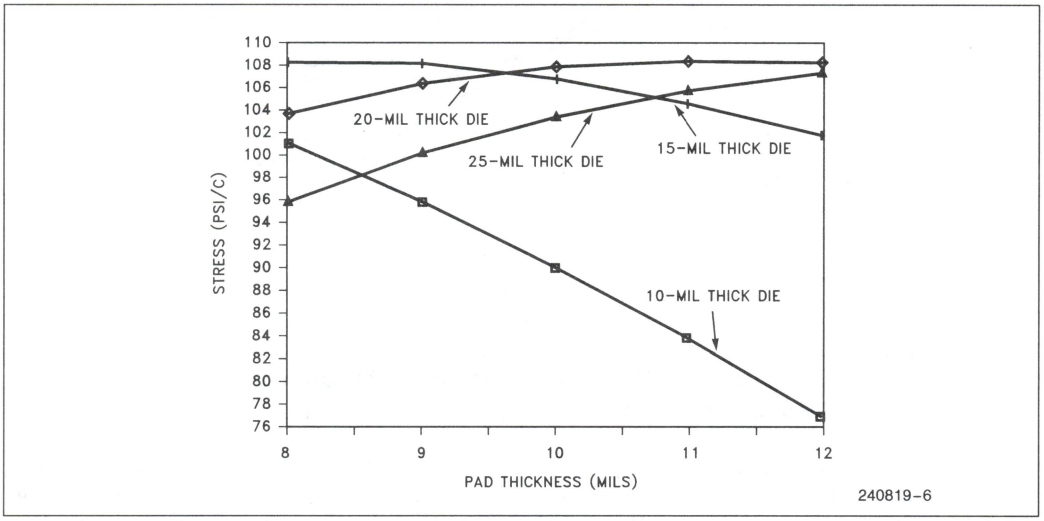


Figure 4-6a. Die Surface Stress Dependence on Pad Thickness

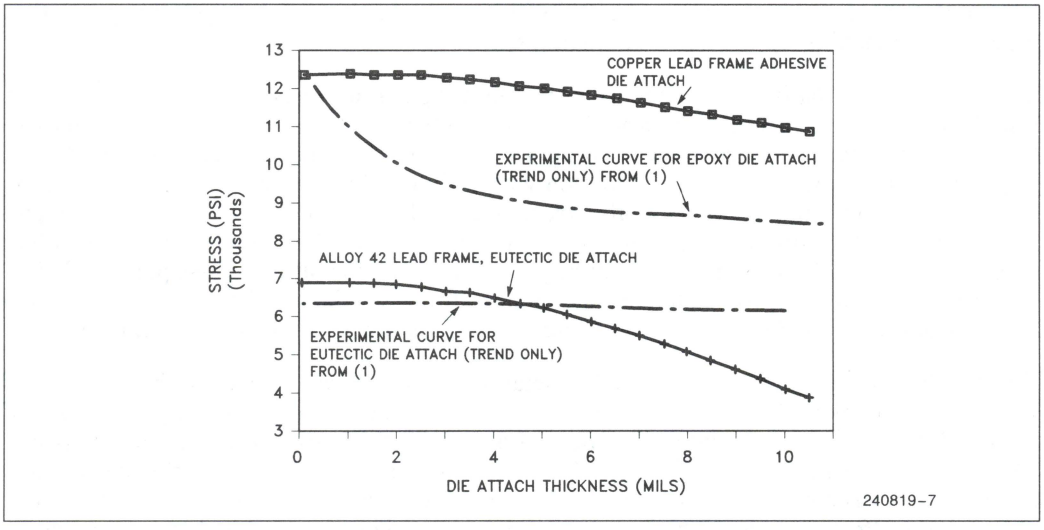


Figure 4-6b. Die Surface Stress Dependence on Die Attach Thickness

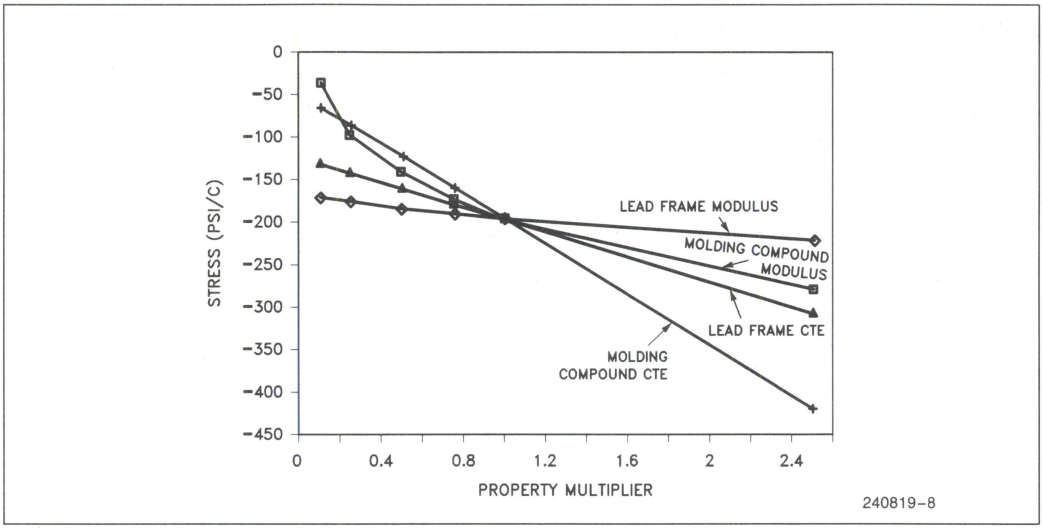


Figure 4-7. Die Surface Stress Variation with Molding Compound and Lead Frame Properties

These stress fields have been calculated using laminated beam theory and thus are applicable to regions of the die, lead frame, and package away from the edge of the laminations. Edge effects are discussed at the end of this section. The stress levels reported here are based on cooldown from the process temperature (T ~ 240°C for die attach, T ~ 170°C for encapsulation), the zero stress state, where thermal stresses arise because of differential expansion of the materials making up the beam laminations.

Shown in Figure 4-6a is the dependence of the die's top-surface stress on die, die attach, and lead frame thickness. Because the lead frame contracts more than the die during cooldown, the laminated beam bows upward, creating a tensile stress on the die's top surface. As the figure illustrates, a thick die in combination with a thin pad acts to reduce the tensile stress level. Interestingly, the converse is also true: A thin die in combination with a thick pad reduces the stress. This seemingly anomalous result is due to the reduction in the bending stress as one layer of the laminated beam begins to dominate the differential expansion. When the two lamina have approximately equal bending stiffnesses–i.e., similar products of elastic modulus and cube of thickness–bowing and top-surface stress in the beam maximize.

This result shows that the "worst case" bimetallic strip effect can be avoided by selection of modulus and thickness values that produce a strong mismatch in the bending stiffnesses of the two layers. Figure 4-6b shows the effect of die attach thickness on the die surface stress. The laminated beam model predicts a reduction in stress as the thickness of the die attach is increased. Experimental data also included in the figure shows that the trends are similar although the effect saturates at higher attach thicknesses. This is probably due to time-dependent stress relaxation effects which are not taken into account in the model. Nevertheless, it is important to note that a die attach thickness of 0.001 to 0.002 in. is sufficient to reduce the stresses induced in the die attach process. This effect is also exhibited in the die attach region; a 2-D FEA model of attach shear stresses shows a similar thickness dependence (see Table 4-10).

Table 4-10. Effect of Die Attach Thickness on Bond Line Shear Stress Level

Die Attach Thickness (in.)	Shear Stress (psi/C)
0.000	102
0.001	33
0.002	33

Material property variations (elastic modulus, expansion coefficient) can produce significant changes in the die top-surface stress. On the one hand, selecting layer elastic moduli to give equal bending stiffnesses will maximize the top-surface stress for the reasons mentioned previously. On the other, when the expansion coefficients of the layers match, no differential expansion develops, and thermal stresses vanish.

Table 4-11 compares top-surface stresses for copper and Alloy 42 lead frame materials. As shown, with the Alloy 42 lead frame, the die level stress is ~ 50% of that for the copper lead frame. While the higher expansion coefficient of copper gives rise to higher process stresses at die attach, the effect is offset following encapsulation because copper and molding compound expansion coefficients are well matched. This effect is discussed later in this section.

Table 4-11. Effects of Lead Frame Material Properties on Die Stress Levels

Layer	Location	Stress (psi)	
		Alloy 42† Eutectic D/A*	Copper† Epoxy D/A†
Die	Top	+5750	+12200
	Bottom	−11600	−19500
Die Attach	Top	+33700	+33700
	Bottom	−33100	−33100
Lead Frame	Top	+6030	+12700
	Bottom	−3940	−2280

*Based on stress-free state of 363°C (eutectic temperature).
†Based on stress-free state of 135°C (epoxy D/A T_g).

NOTES:
1. Layer thicknesses: die, 0.015 in.; die attach, 0.001 in.; lead frame, 0.010 in.
2. Cooldown end point temperature: 20°C

The effect of die attach material properties on die stress has also been explored through both modeling and measurement. Tables 4-12 and 4-13 show experimental stress data from two separate tests for different adhesive die attach materials. This data indicates that top-surface stress can vary by almost an order of magnitude, depending on the adhesive selected (polyimide, epoxy, or thermoplastic). The greatest effect is found for materials with a low glass transition temperature.

Table 4-12. Experimental Values of Die Top-Surface Stress Components Following Die Attach

Die Attach Material	σxx (psi)	σyy (psi)	σxy (psi)	σmax (psi)
Epoxy (Ablebond 84-1) 8 Samples	11600 ±1020	10800 ±1220	90 ±604	12000 ±1080
Polyimide (Ablebond 71-1) 19 Samples	26400 ±13700	24200 ±10000	−89 ±1690	29300 ±12300

Table 4-13. Effect of Different Die Attach Material Properties on Stress Level

Die Attach Material	Corner		Center	
	σxx (psi)	σyy (psi)	σxx (psi)	σyy (psi)
Thermoplastic (M & T)	3800 ±2000	3300 ±1900	3700 ±2300	2200 ±2000
Epoxy (Ablebond 84-1)	6700 ±1700	4800 ±1600	10300 ±1300	9500 ±1200
Polyimide (Ablebond 71-1)	40400 ±7100	34400 ±7000	45000 ±12500	38300 ±8500

Stresses in the package following molding have been calculated using the laminated beam analysis, and the results are displayed in Figures 4-7 through 4-9. Thus, increasing molding compound modulus and/or coefficient of thermal expansion serves to raise the compressive stress on the surface of the die (Figure 4–7) and raise the tensile stress in the molding compound above the surface of the die (Figure 4-8) and below the die paddle (Figure 4-9). The sensitivity of stress changes to each of the property changes is indicated by the slope of each of these curves. As seen in Table 4-8, the difference in the expansion coefficient between the silicon and the molding compound is of the order of 15 $(MC)^{-1}$. Qualitatively, this differential gives rise to post-cooldown stresses that are compressive in the die and tensile in the molding compound. Although the compressive stress may contribute to die reliability, the corresponding stress in the molding compound may lead to package cracking, particularly if the package is thin. Comparison of the actual stress with the fracture strengths given in Table 4-9 will enable the designer to determine the amount of margin available in a design.

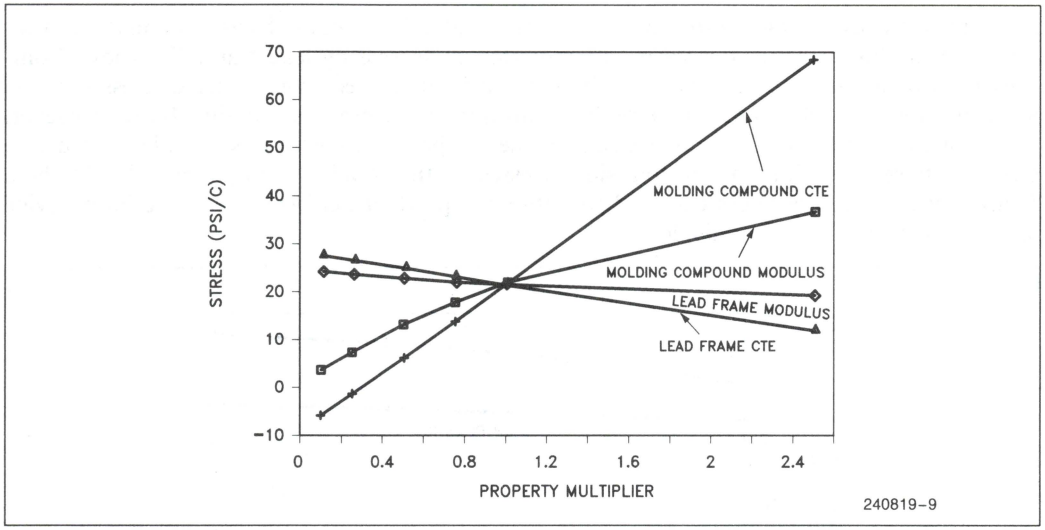


Figure 4-8. Variation of Plastic Stress above Die Surface with Molding Compound and Lead Frame Properties

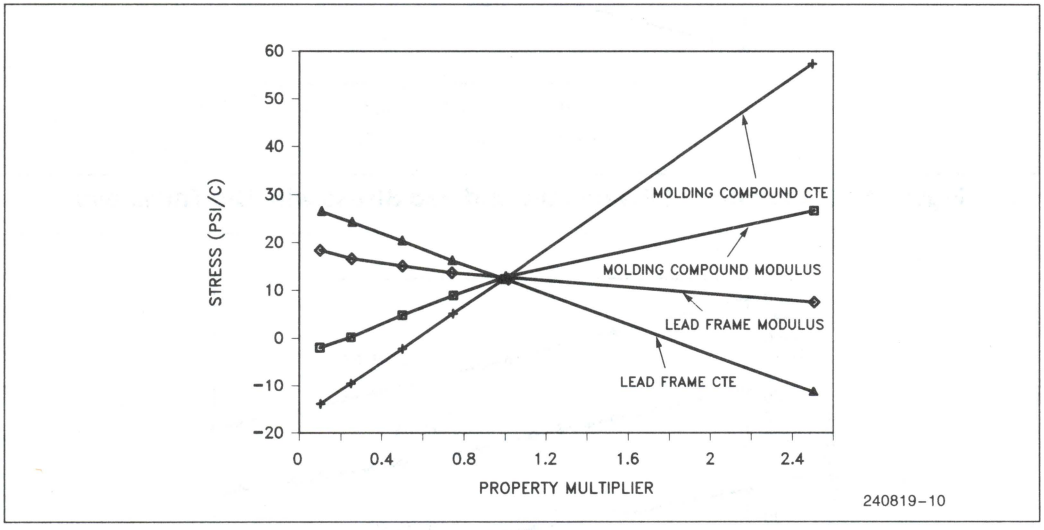


Figure 4-9. Variation of Plastic Stress below Die Paddle with Molding Compound and Lead Frame Properties

Package geometry effects on stress are illustrated in Figures 4-10 through 4-13, which include variations in package die, die attach, and lead frame thicknesses, as well as pad depress. The figures show that decreasing package thickness or increasing die thickness leads to reduced compressive stress on the die surface and increased tensile stress in the molding compound

adjacent to the die surface. Further, increasing die attach thickness has the same die-to-lead frame decoupling effect as decreasing its modulus or decreasing lead frame thickness. Compressive stresses at the top surface of the die can be increased, while tensile stresses in the adjacent molding compound can be reduced through pad depress (see Figure 4-13). However, tensile stresses in the compound adjacent to the die pad will increase, so a balance must be struck between top-side and bottom-side stresses in the molding compound. Use of these figures by package designers can lead to optimized product performance, since both device and package can be made reliable.

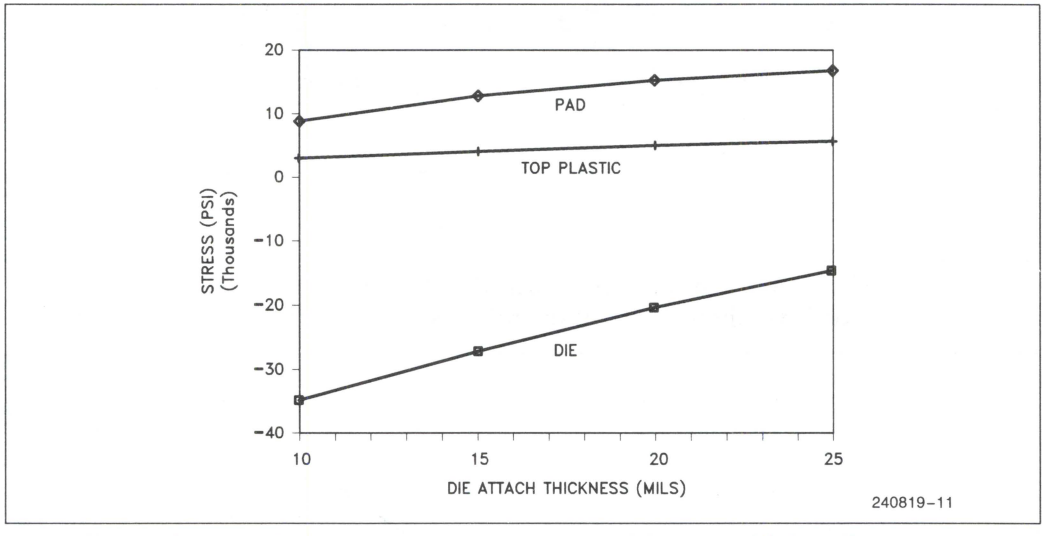


Figure 4-10. Variation of Plastic, Die and Pad Stress with Die Thickness

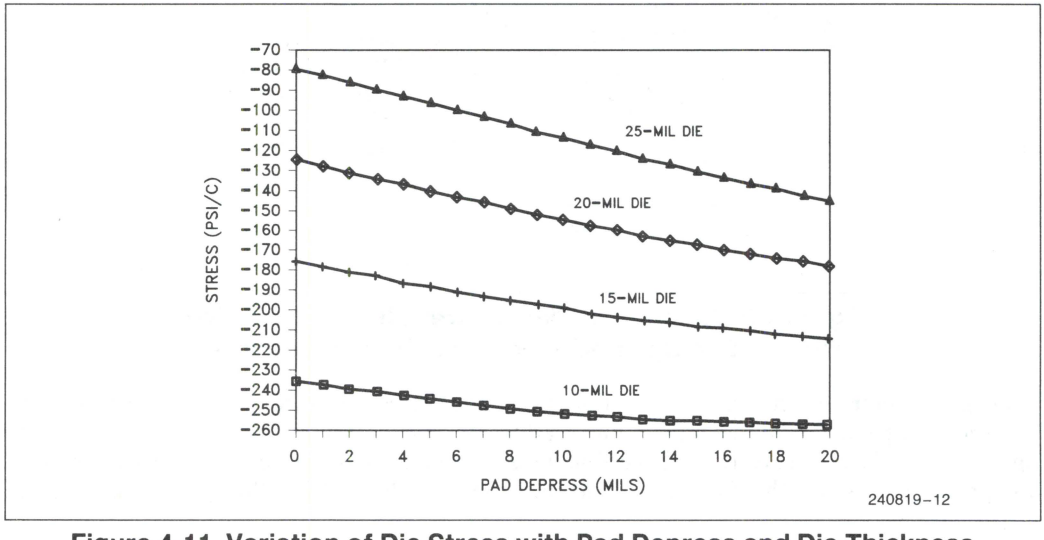


Figure 4-11. Variation of Die Stress with Pad Depress and Die Thickness

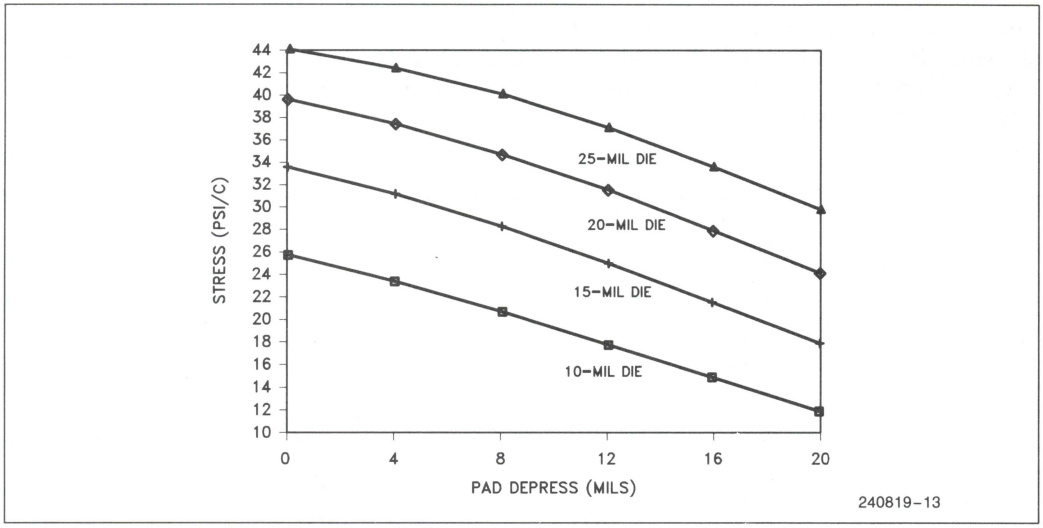


Figure 4-12. Variation of Plastic Stress above Die Surface with Pad Depress and Die Thickness

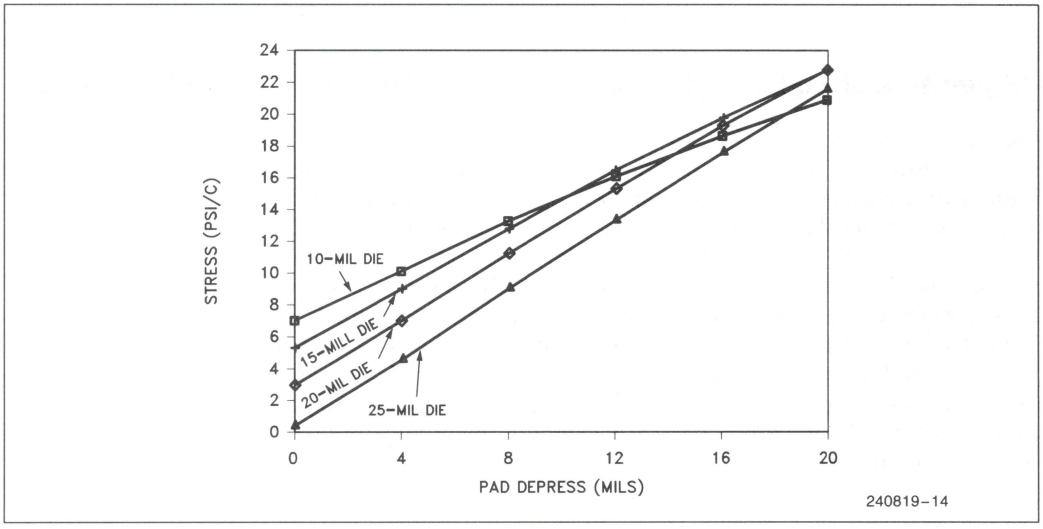


Figure 4-13. Variation of Plastic Stress below the Pad with Pad Depress and Die Thickness

Of continuing concern to design and process engineers is the effect of die size on the integrity and reliability of die attach. In fact, 2-D and 3-D FEA stress models confirm that once the die exceeds a critical size–usually about 10 times the die thickness (i.e., 0.200 in. for a die 0.20 in. thick)–stress magnitudes and distributions near the edge do not change. The reason for this seemingly anomalous result is that the characteristic length of the edge effect is governed by the thickness of the die or substrate (lead frame, plastic or ceramic base, etc.).

For the case of a die attached to a lead frame, the die thickness has the greatest effect. As shown in Figure 4-14, which illustrates the die attach shear stress distributions for die sizes varying from 0.190 to 0.390 in., the edge value is the same, although the distributions into the interior vary somewhat.

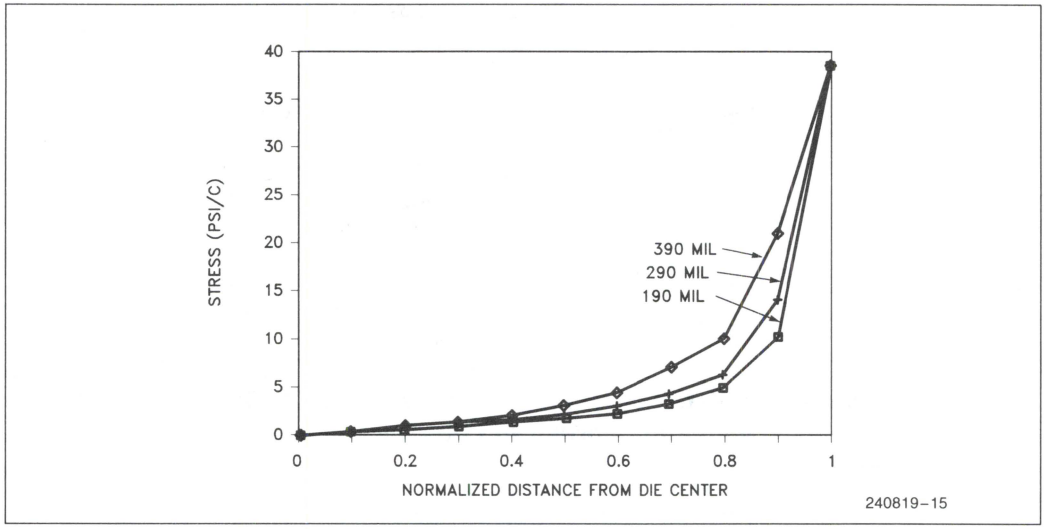


Figure 4-14. Shear Stress Distribution on Die Surface for Three Die Thicknesses

On an even larger scale, the 3-D FEA model of die attach shear stresses for the case of a silicon substrate 1.5-in. square attached to an alumina substrate shows that the effect is limited to a border region approximately 0.300 in. in width (see Figures 4-15a and 4-15b). Again, the border dimension is governed by the die thickness (0.025 in.). Attach thickness is 0.0025 in. and Al_2O_3 package base thickness is 0.077 in. In addition, formulas for bond stresses based on beam-on-elastic foundation analyses support the results obtained numerically (see Reference 2). Reports of die cracking and poor die attach reliability as the die size is increased beyond 0.500 in. suggest that the assumptions used in the model–i.e., constant thickness and material properties along the entire bond line–are not readily achieved in practice. Improvements in die backside preparation, in dispensing of the attach material, and in the drying and baking processes are generally required before the "small-die" performance levels can be reached.

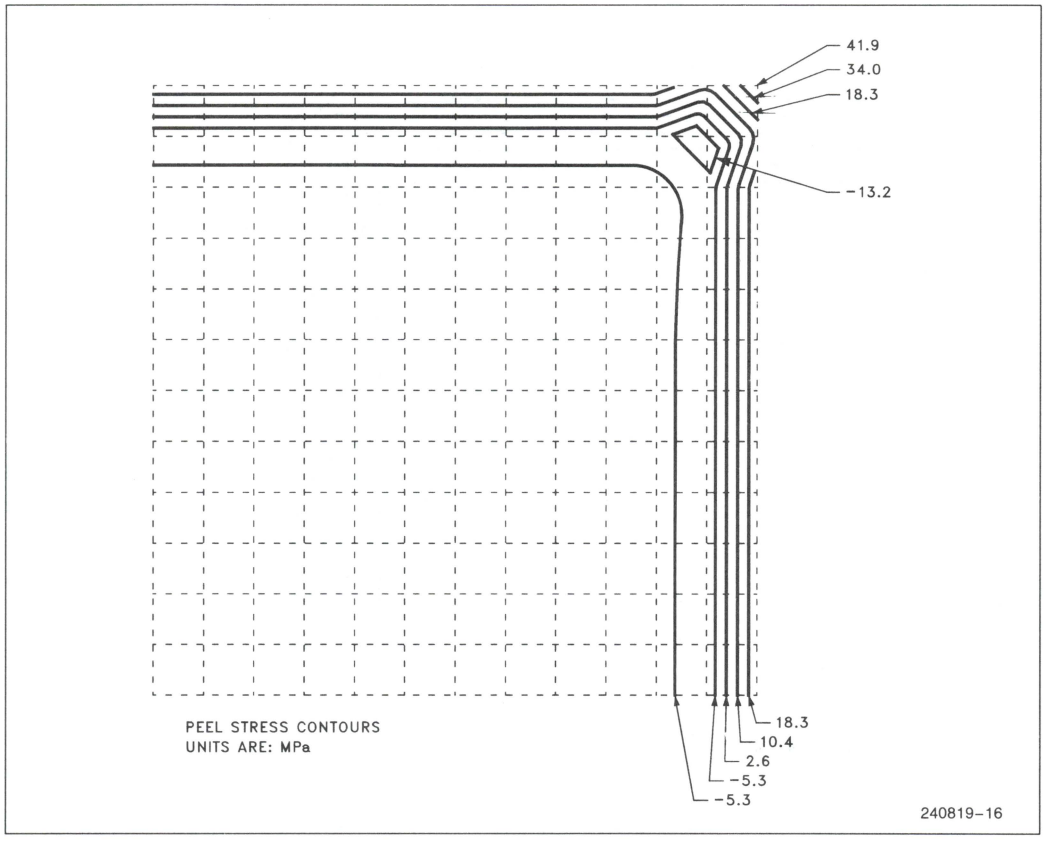


Figure 4-15a. Peel Stress Contours

Figures 4–15a and 4–15b show peel and shear stress contours in the adhesive attaching a silicon substrate to Al_2O_3 package cavity.

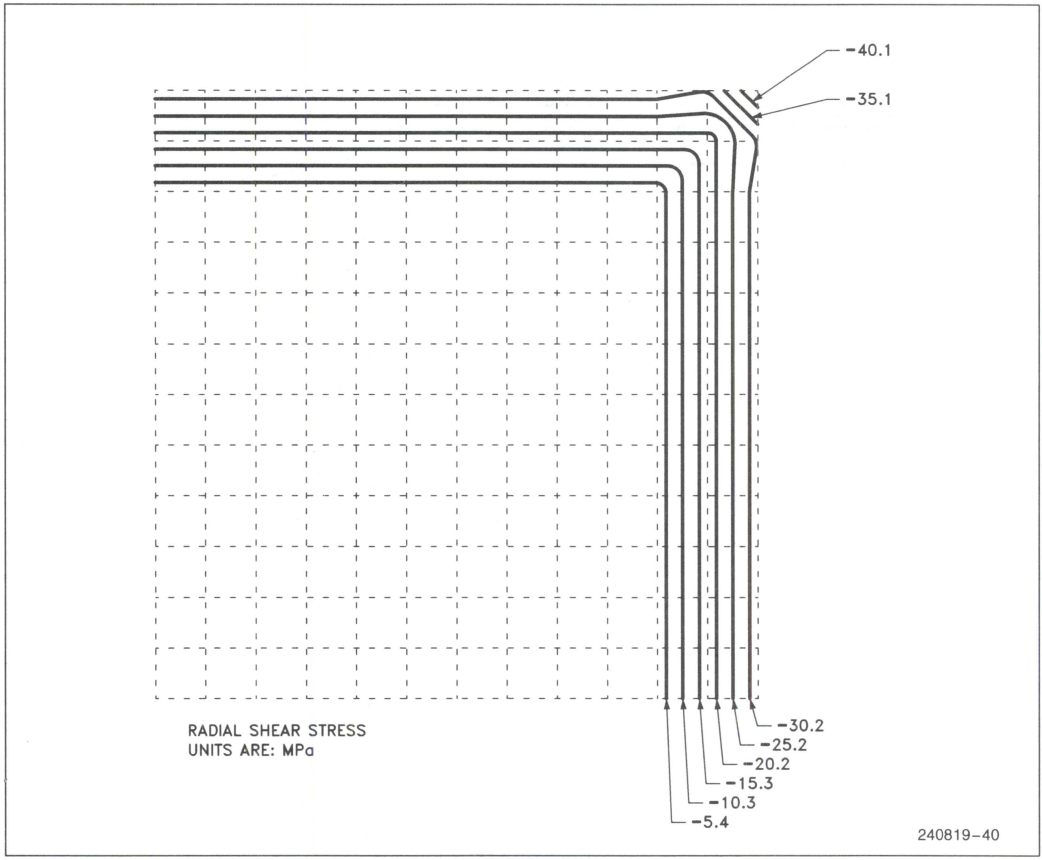


Figure 4-15b. Radial Shear Stress Contours

INTERFACIAL STRESSES AND DELAMINATION

Numerous contributions have been made toward an understanding of the mechanisms associated with delamination of the encapsulant from the elements in the package (die, lead frame, etc.). Chief among these are the articles by Fukuzawa, et al. (see Reference 3), Belton et al. (Reference 4), Steiner and Suhl (Reference 5), and Bhattacharyya, et al. (Reference 6).

The key events or process steps leading up to delamination can be incorporated into a reasonably coherent picture on the basis of information presented in these references. Interfacial bonding occurs during cooldown from the mold and cure temperature, usually close to T_g, the glass transition temperature of the molding compound (see Figure 4-16a). Tensile stresses develop across the interfaces during heatup above T_g as part of the solder reflow process (see Figure 4-17a). Delamination sites initiate and grow under the proper set of environmental parameters, i.e., temperature, pressure, and sorbed moisture. Each of the process steps is reviewed in greater detail below to highlight the roles played by the important parameters during that step.

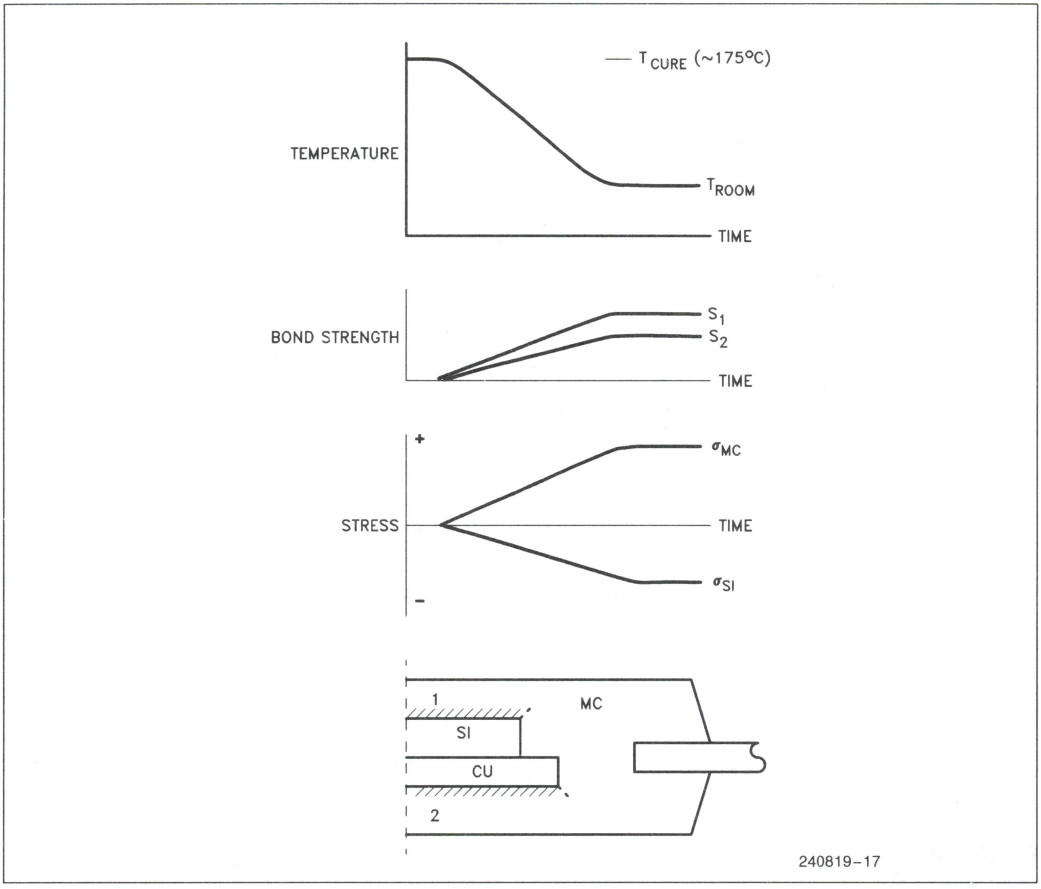


Figure 4-16. Cooldown Process

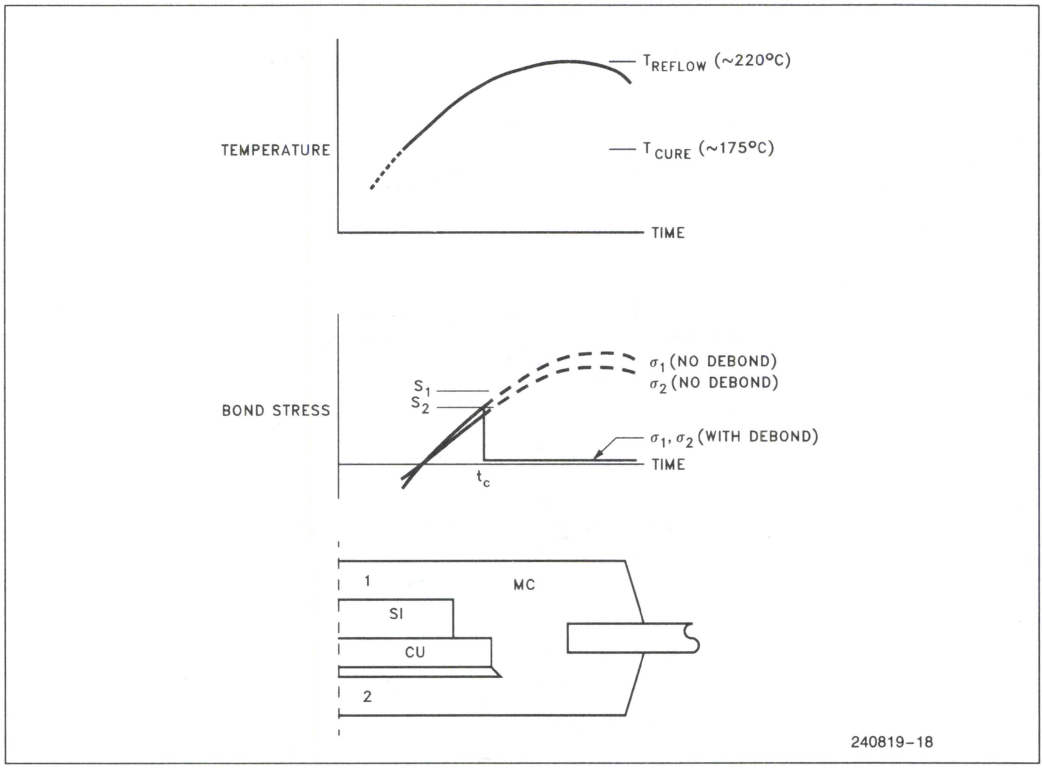


Figure 4-17. Reflow Process

Cooldown from T_g

In addition to bulk cross-linking, thermal stresses develop because of the differential thermal expansion (contraction) between the encapsulant and internal elements. As Figure 4-16c shows, this thermal stress field–tensile in the bulk encapsulant, compressive in the enclosed elements–is favorable to the development of a strong interfacial bond. The exact nature of the bond–chemical, mechanical, or other–is not fully understood. However, a favorable combination of temperature and time is expected to maximize the bond strength. Room temperature measurements indicate relatively strong bonds between encapsulant and silicon (> 1 Ksi) and somewhat weaker bonds between encapsulant and lead frame (see Figure 4-16b). Surface treatments (oxidation) and design features such as anchor wells and/or holes enhance the encapsulant/lead frame bond strength, although probably not above that of the encapsulant/silicon bond. Of particular interest in recent years is the influence of sorbed moisture on the bulk and interfacial properties of the encapsulant and internal elements. Measurements to date do not demonstrate any strong trends, although some interfacial bond strength degradation is suggested.

Heatup above T_g

As the package temperature is raised above T_g during the solder reflow process, the thermal stress state passes through its neutral point and then reverses sign; i.e., the bulk encapsulant stress becomes compressive, the internal elements tensile. The interfacial bond is placed in tension, and delamination will occur first at sites where the bond strength is exceeded. Other things being equal, an isotropic stress state will initiate delamination at the encapsulant/lead frame interface because of its intrinsically lower inherent strength (see Figure 4-17b). Delamination stability/instability will depend on the stress state and the intrinsic fracture resistance of the bond; indeed, some analogy may be made to crack initiation and propagation at a bimaterial interface with known fracture toughness.

The presence of moisture can complicate the delamination process significantly, adversely affecting mechanical properties such as modulus and thermal expansion coefficient, and reducing interfacial bond strength. In addition, the moisture trapped at and near the interfaces may be in the liquid phase at the start of the heatup cycle and be driven to saturation pressure levels associated with reflow temperatures (> 300 psi; see Figure 4-18b), since there is insufficient time for moisture migration to the outside of the package. According to numerous independent measurements, bulk diffusivity decreases with moisture concentration. As a result, moisture discharge occurs more slowly than moisture uptake, and the reflow temperature profiles do not allow adequate time to prevent or reduce saturation pressure build-up.

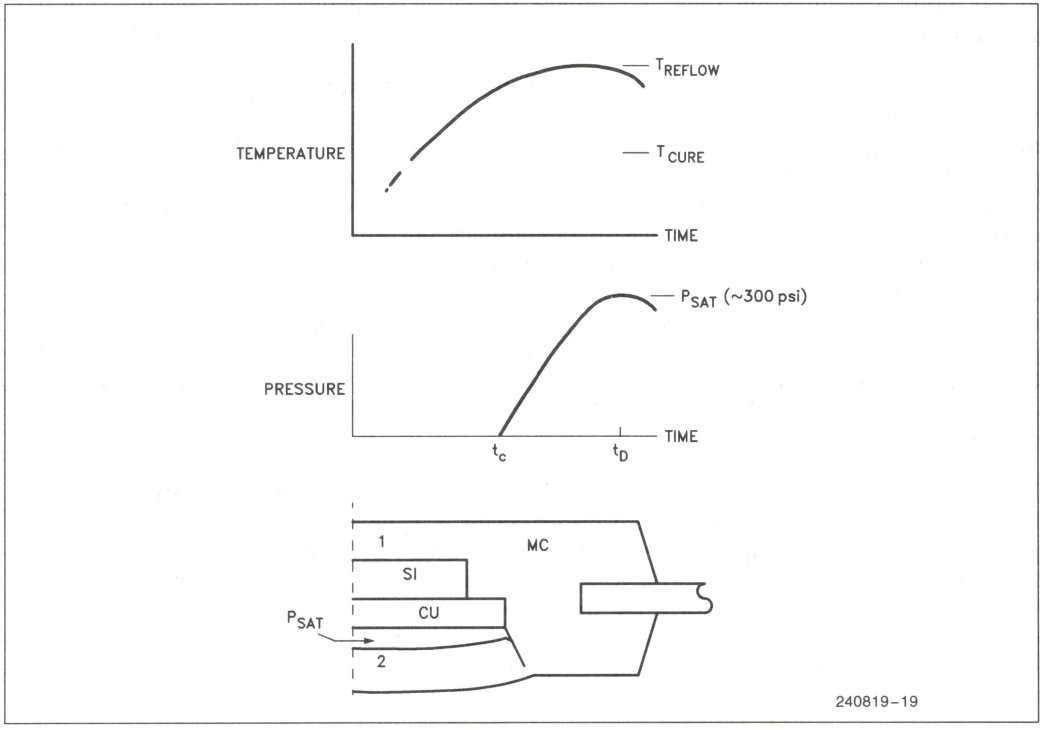


Figure 4-18. Pressure Buildup during Reflow

As discussed in References 3 and 6, the size and shape of the package and its contents play an important role in the integrity and reliability of the interfacial bonds. When the package is thin, and the die and die paddle both large, there is the potential for the development of high tensile stress in the bulk encapsulant adjacent to the bottom corner of the die paddle or at the top corner of the die during the reflow process. This stress results primarily from the delamination caused by the heatup-induced interfacial tensile stresses in combination with the saturation pressure build-up at the interface when sufficient moisture is trapped in the encapsulant to act as a source of high-pressure water.

As explained in References 3 and 6, the governing geometric parameter is L/h, the ratio of the die or die paddle size to the thickness of the package beneath the paddle or above the die. This parameter serves as a multiplier of the saturation pressure for estimating the stresses in the encapsulant at the critical corner zone. Theoretical considerations suggest that the encapsulant should not fracture as long as $L/h < 6$; above this level, the encapsulant fractures, and a crack propagates from the corner outward to the free surface of the package. Data compilation (see References 7 and 8) suggests that $L/h < 5$, although the linear relation between L and h is confirmed. Under extreme conditions, the failure is accompanied by a snapping sound and has been dubbed the "popcorn effect". Bulging of the package surface above the delaminated zone (see Figure 4-18c) reinforces this analogy. An adequate supply of high-pressure water is necessary to support the bulging. Moisture weight gains of 0.1%, said to be the critical level for the popcorn effect, are more than adequate for bulge heights of 0.001 in. in a 0.200-in. delamination zone. Not only is the bulge cosmetically unacceptable, but it is generally accompanied by cracks from the die/die paddle edge to the outside of the package.

Selection of material properties, control of the environment, and careful design can reduce, if not prevent, delamination and associated failure mechanisms in the package. Increasing delamination strength is of prime importance and can be achieved through both mechanical and chemical means. Since die-paddle cracking is most prominent, treatment of the metallic surface–oxidizing, roughening, or designing of anchor well or through-holes –is receiving considerable attention. Results are still preliminary but are encouraging. Modification of material properties to achieve higher encapsulant fracture strength and to reduce moisture uptake is ongoing, although major breakthroughs have not been reported or expected. There is little enthusiasm in the systems design arena to raise the package profile; indeed, there is pressure to reduce package thickness (i.e., h) even further. As a result, it will be important to limit die and paddle sizes as much as possible. Even this objective is thwarted by device designers who seek to add more functionality to their product, leading to an increase in device size (i.e., L).

Because of the key role played by trapped moisture in the internal pressurization effect, keeping the weight gain below 0.1% is critical. This is achieved through the "bake and bag" process before product shipment. Desiccated barrier bags have been shown to provide at least six months' protection against critical moisture build-up in the package. Parts used beyond the storage life can be rebaked prior to reflow to recover safe moisture levels. Until the enhancements discussed earlier can be accomplished, the bake and bag steps will be an important part of the process for reliable board-level assembly.

Bond Stresses

In addition to the mechanical and metallurgical stresses developed during the wire-bonding process, encapsulation and environmental stresses subsequent to bonding can contribute to degradation of the interconnection. Reliable first and second bonds can be ensured by bonding within the process windows for force, power, time, and temperature. Excursions beyond these windows are minimized through regular process monitors such as bond pulls. Both pull strength and failure mechanism criteria must meet specifications. In particular, no cratering failures are acceptable even if pull strength criteria are met, since craters indicate excessive force during bonding, which could lead to reliability problems in the field.

During encapsulation, wire sweep may occur if wire lengths are too great or if drag during molding flow is excessive. Current mold gate designs provide low drag flow patterns, and X-ray monitors are used to confirm process stability. Wire diameter and length design rules are strictly enforced to ensure that there is adequate mechanical stability of the bond arch to resist the drag forces. Development of new package designs includes analysis and experiment to ensure that wire sweep is minimized.

In plastic packages, delamination at the interface between the molding compound and silicon or lead frame can cause high stresses at the first or second bond location, because the differential thermal expansions must be accommodated across the bond itself. The delamination generally results from temperature cycling of packages with trapped moisture. To suppress the adverse effects of delamination, selection of materials with enhanced interfacial adhesion and the design of lead frames that feature additional mold compound locking characteristics have proven to be effective. Three-dimensional FEA models are used to guide and optimize the designs. For packages that are particularly moisture-sensitive, shipment of prebaked product in sealed moisture-proof bags with desiccant ensures that delamination is minimized and operation of the assembled part will be reliable.

Compliant Leads and Solder Joint Fatigue

With the advent of surface mounted packages, solder joint integrity became an issue of considerable concern. It was found that solder joints on leadless ceramic packages measuring more than 0.5 in. on a side could survive only a few hundred temperature cycles (Condition B, −55°C to +125°C) when the packages were surface mounted to FR4-type circuit boards. The addition of compliant leads to these packages has extended the life considerably and is now used in the design of all new surface mounted packages.

As a means of experimentally evaluating the in situ stiffnesses of leads on packages surface-mounted to boards, the straddle board method has proved to be a very useful tool (see References 12, 13 and 15). As shown in Figures 4-19 and 4-20, the straddle board consists of a slotted, double-sided epoxy-glass FR-4 board that is patterned for corner leads; all other package leads are removed.

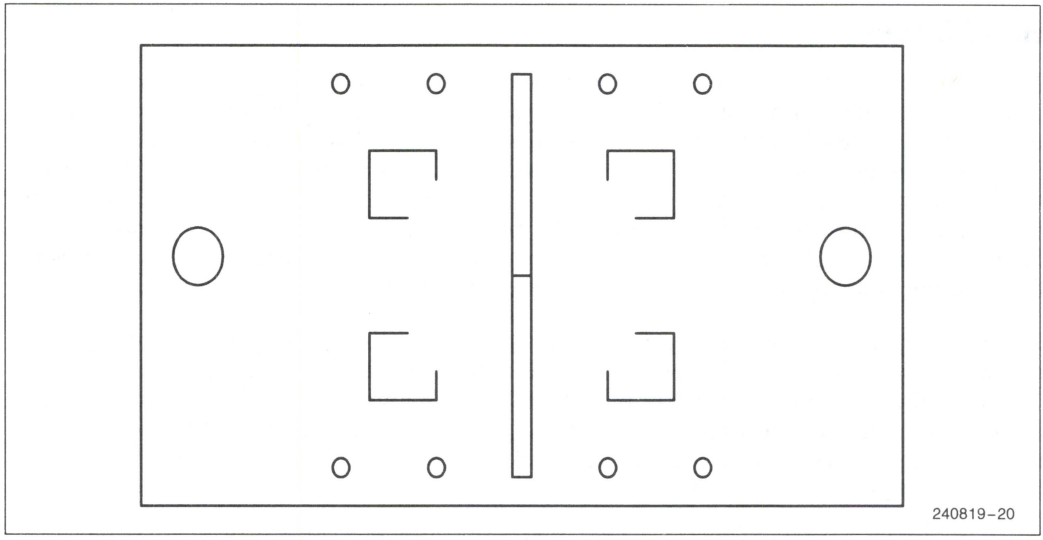


Figure 4-19. Lead Stiffness Straddle Board

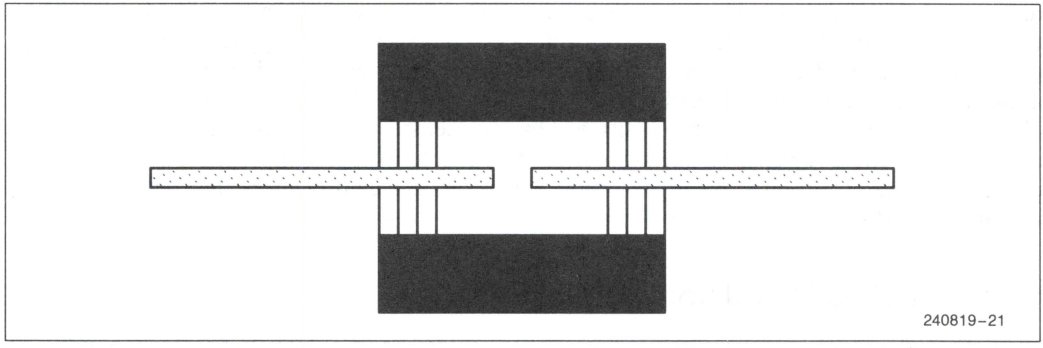


Figure 4-20. Straddle Board with Two Packages in Place

Units are mounted on both sides of the board using production-level processes and specifications for each package. The board is mounted vertically in a tensile test set-up such as a materials test system (MTS), and the narrow sides of the slot are cut, separating the two ends of the package. The MTS is fitted with a 200-lb. load cell and a 6-in. displacement actuator. This allows the straddle board to be tested with a 0.020-in. displacement, 0.010 in. in the tensile cycle and 0.010 in. in the compressive cycle. These values were chosen to span the lead displacement experienced during temperature excursions from $-65°C$ to $+150°C$ (MIL-STD-883C T/C [C]).

A total cycle time of five seconds was used with a maximum load range of 0.8-8 lb., depending on the package type and lead count. As Figure 4-21 shows, leads are loaded in both lateral and transverse directions (i.e.; In the plane and normal to the plane of the lead bend). Twenty-five samples per lead count per direction were evaluated. Once the board was mounted, three full cycles were run, and the force vs. deflection curve was recorded. The linear portions of the loading and unloading curves were used to determine the lead stiffness. A typical hysteresis curve is shown in Figure 4-22.

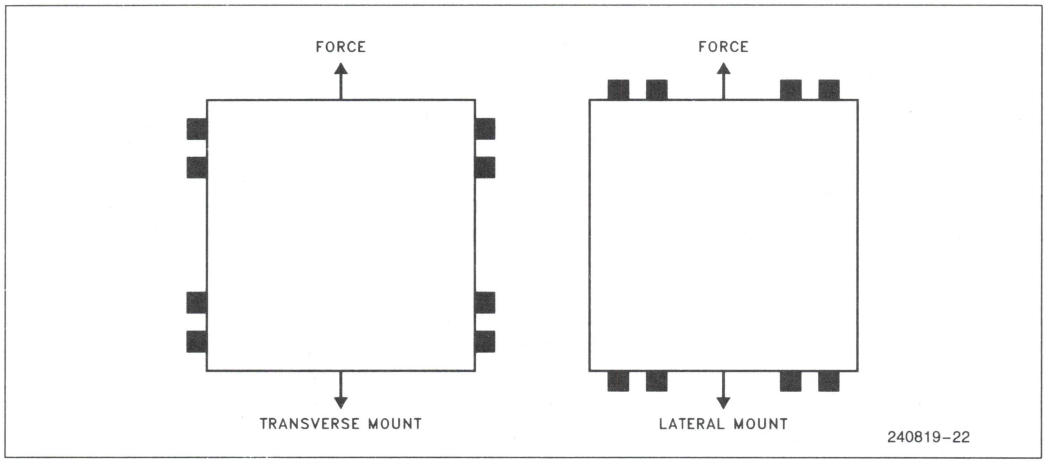


Figure 4-21. Orientation of Applied Load

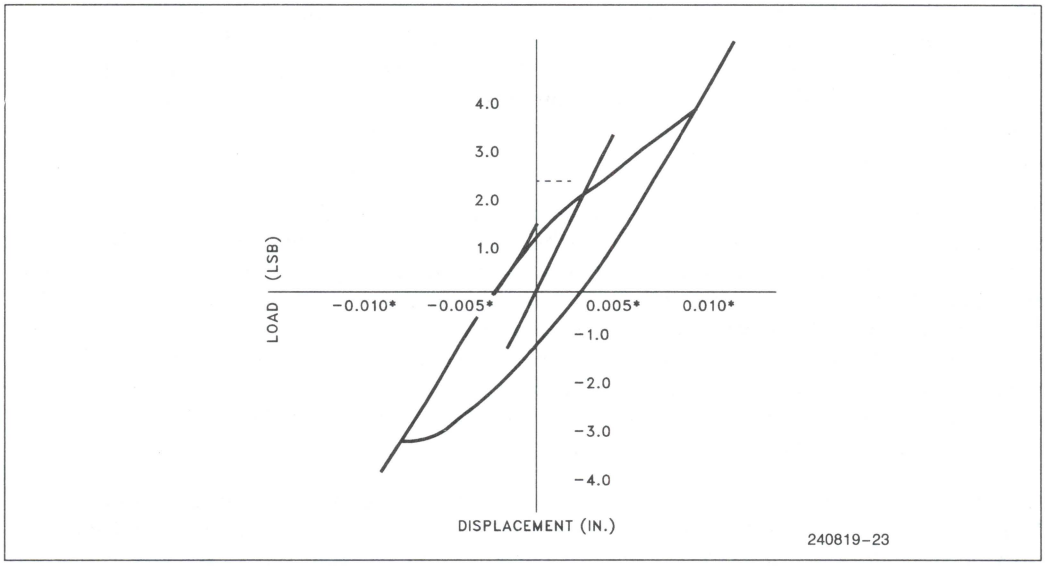


Figure 4-22. Lead Stiffness Determined from Hysterisis Curve

Designing leads with adequate compliance is now recognized as an important element of overall product design, and mechanical modeling has proved to be a useful design tool. Lateral and transverse lead stiffnesses were calculated for PLCC, cerquad, and PQFP packages using the ANSYS 3-D elastic beam element option (see Reference 14). The calculated stiffness for each type of package was matched to the value obtained from the straddle board measurements by locating the point on the lead where agreement was reached. In all cases, the point lay within the solder joint, in agreement with physical expectations.

Of particular interest were the boundary conditions imposed by the solder joint on the foot of the lead. In the lateral direction, the solder volume is adequate for the joint to provide built-in support to the lead foot (zero rotation). However, in the transverse direction for the PLCC and cerquad packages, the J-bend lead stiffnesses are large enough to produce inelastic deformations in the solder joint. As a result, the joint acts like a pinned support (free rotation). In all cases, the PQFP gull-wing leads are sufficiently compliant for the solder joint to act as a built-in support. This result suggests that reducing lead stiffness will significantly reduce solder joint stresses and associated creep and fatigue. Experimental data recently reported in Reference 3 supports this hypothesises.

Because of the contribution of lead stiffness to the level of stress in the solder joint when there is thermal mismatch between package and board, a comprehensive list of in situ lead stiffness values is provided in Table 4-14. All surface mounted packages currently used for Intel products (TSOP, PLCC, cerquad, PQFP and CQFP) are listed in the table. For these packages both translational and rotational stiffness components are given. The translational stiffness is defined as the force in pounds created by a displacement in inches applied at the solder joint in the direction of interest, the remaining force and rotation components being zero. These stiffness components are important when the thermal mismatch creates differential displacements which must be accommodated along the leads. The rotational stiffness is defined as the moment in inch-pounds created by a rotation in radians applied at the solder joint about the axis of interest, all other moments and displacement components being zero. These stiffness components are important when thermally induced differential rotations are imposed at the ends of the leads.

The magnitude of the stiffness components are useful in making comparisons of the level of stress or strain induced in the solder joint by various package types; high lead stiffness will generate high solder stresses, etc. Experience to date indicates that in situ translational lead stiffnesses on the order of 100 lb/in. or less produce excellent solder joint reliability (see References 11 and 13). Even lead stiffnesses above this level are acceptable although they have less margin than the more compliant leads. With reference to Table 4-14, the x- and y-components of the gull-wing leads on 0.025 in. centers (PQFP and CQFP) fall into this category. The z-components are always large and demonstrate the importance of minimizing board flexing, which generates these z-components.

Under certain conditions, stresses in the lead may be large enough to cause reliability problems in the lead prior to those arising in the solder joint. The last six columns in Table 4-13 provide indicators of lead stress levels for current Intel package types. When the stress is displacement driven, the first three of these columns give the level of stress produced by a differential displacement of 1 milli-inch across the lead under the same boundary conditions as those for the equivalent translational stiffness component; the rotation driven stresses appear in the last three columns and show the stress produced by a 1 milliradian rotation mismatch for boundary conditions equal to those for the equivalent rotational stiffness component. In general, there is a correlation between the lead stiffness and the lead stress; the greater the stiffness, the greater the stress. Thus, PQFP and CQFP leads experience relatively low stresses for a specified displacement mismatch. However, in the case of z-component mismatch, lead stresses may be high enough to cause reliability jeopardy. Minimizing board flexing will reduce this jeopardy.

To assist in visualizing the stiffness and stress entries in Table 4-14, Figure 4-23 has been prepared. The gull-wing lead of the PQFP has been used for reference. In all entries, the center line represents the lead profile in the plane of interest. The heavy line represents the displacement profile associated with the displacement or rotation component indicated at the point on the lead connected to the solder. The line connected by shading to the undeflected profile shows the distribution of the bending stress along the lead. In general, the maximum value is at or near the solder connection point; however, for displacements along (or rotations about) the z axis, the bending stress maximizes at the package body. As mentioned previously, z-component displacements may generate high lead stresses; Figure 4-23 suggests that the package body is the site of maximum stress and damage in the lead.

Table 4-14. Surface Mount Package Lead Stiffness

Package Type	Lead Stiffness Components						Maximum Lead Stresses					
	Trans. Stiffness (lb/in.)			Rotation Stiffness (in.-lb/rad.)			Trans. Stresses (Ksi/m in.)			Rot. Stresses (Ksi/m rad.)		
	Kx	Ky	Kz	Kθx	Kθy	Kθz	σx	σy	σz	σθx	σθy	σθz
TSOP (I)	1900	2560	9730	0.579	0.435	0.115	514	521	1660*	7.89	9.55	1.78*
TSOP (II)	3820	18800	19500	4.42	0.869	0.704	514	990	1660*	15.1	9.55	2.86*
PLCC 44L	323	1250	7750	1.82	0.379	1.03	43.3	59.1	335	1.81+	6.65	1.56+
PLCC 68L	187	1190	8813	1.03	0.166	0.641	43.7	89.1	474	3.08+	6.99	2.60+
Cerquad	120	1330	6090	1.05	0.0919	0.616	42.8	119	591	3.79	7.45	1.45
PQFP	39.8	85.9	955	0.245	0.133	0.0468	30.4	35.9	281*	1.98	2.05	0.438*
CQFP	9.05	23.0	250	0.361	0.0132	0.0232	16.0	24.8	173*	2.39	1.62	0.342*

DEFINITIONS:
Kα—Force in lbs. needed to produce a displacement in in. in the α direction at the solder joint, all other forces and rotations = 0.
Kθα—Moment in in.-lbs. needed to produce a rotation in rad. about the α axis at the solder joint, all other moments and displacements = 0.
σα—Maximum lead stress in Ksi due to a 0.001 in. displacement in the α direction at the solder joint, all other forces and rotations = 0. Unless otherwise noted, maximum stress occurs at the solder joint.
σθα—Maximum lead stress in Ksi due to a 0.001 rad. rotation about the α axis at the solder joint, all other moments and displacements = 0. Unless otherwise noted, maximum stress occurs at the solder joint.
x—Outward normal to the edge of the package in the plane of the unformed leadframe.
y—Tangent to the edge of the package in the plane of the unformed leadframe.
z—Perpendicular to the plane of the unformed leadframe.

NOTES:
*Maximum at the package body.
+Maximum at the site of lead width reduction.

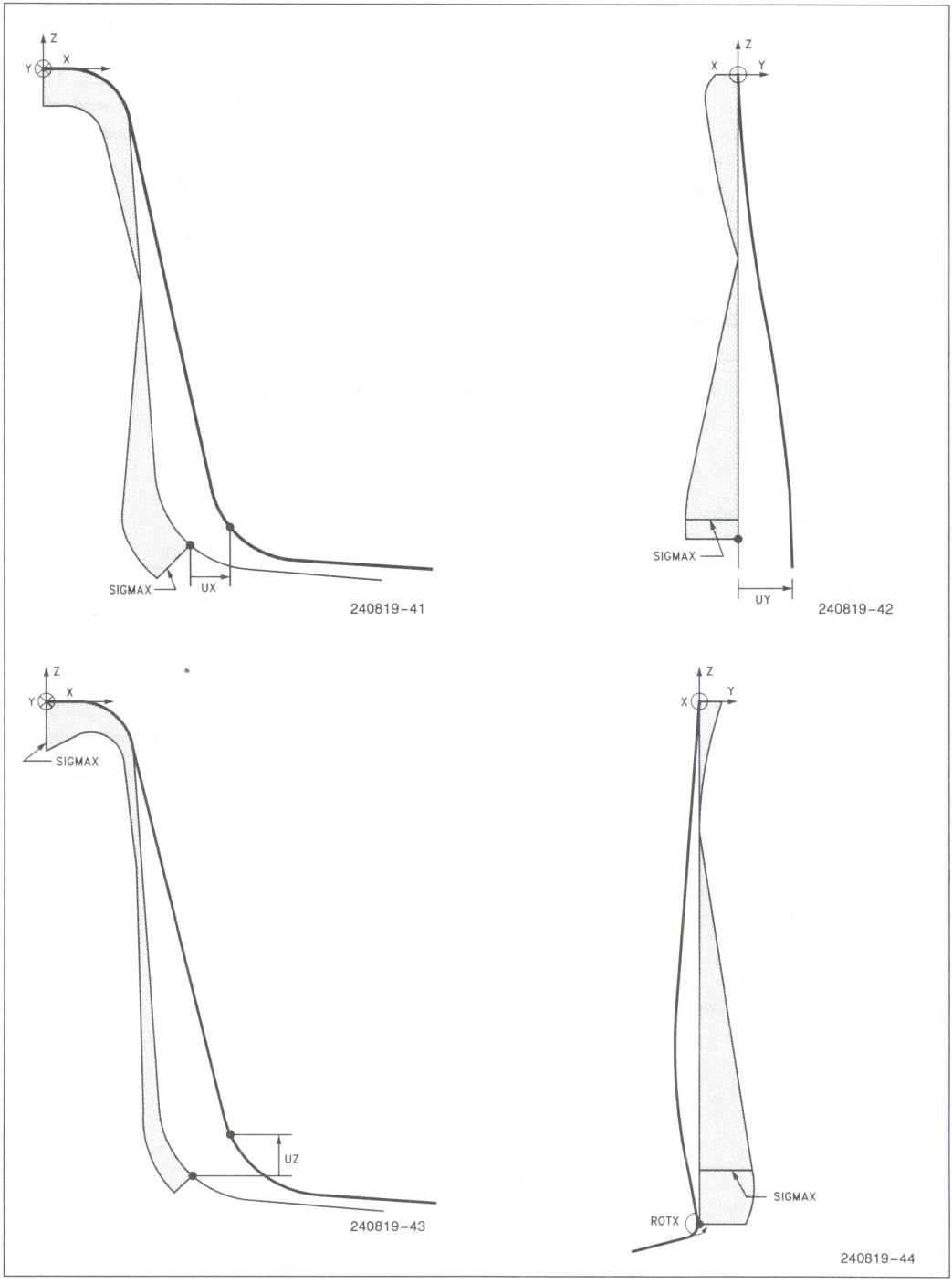


Figure 4-23. Stress Distribution along a PQFP Lead

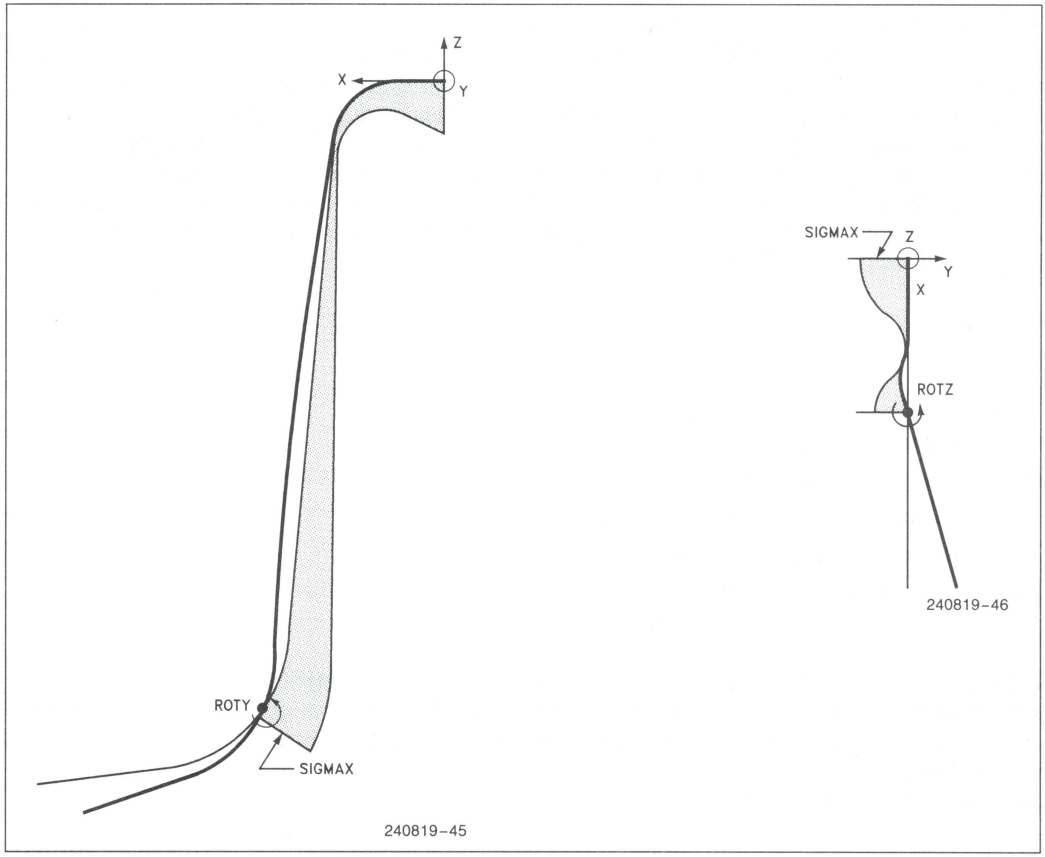


Figure 4-23 (Continued)

IC PACKAGE THERMAL CHARACTERISTICS

Importance of Thermal Management

Thermal management of an electronic system encompasses all the thermal processes and technologies that must be utilized to remove and transport heat from individual components to the system thermal sink in a controlled manner.

Thermal management has two primary objectives. The first is to ensure that the temperatures of all components are maintained within both their functional and maximum allowable limits. Functional temperature limits provide the temperature range within which the electrical circuits may be expected to meet their specified performance requirements. Operation outside this range may result in degraded machine performance or logic errors. The maximum allowable temperature limit is the highest temperature to which a component or part of a component may be safely exposed. Operation above the maximum allowable temperature limit may result in actual physical destruction of the component or irreversible changes in its operating characteristics.

The second objective of thermal management is to ensure that distribution of component operating temperatures satisfies reliability objectives. Although failure to meet this objective may not be as readily apparent as failing to remain within maximum temperature limits, in the long run it can be equally costly. Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on device operating temperature. The exact relationship between failure rate and temperature depends upon the packaging materials and processes, and the failure mechanism in operation. This relationship can be illustrated for changes in device characteristics resulting from chemical or diffusive processes by using a normalized failure rate defined by an Arrhenius equation:

$$\theta_n = \frac{\theta_T}{\theta_{Tr}} = \text{Exp}\left[(E_A/k)\,(Tr^{-1} - T^{-1})\right] \quad (1)$$

where:

θ = Failure rate

θ_n = Normalized failure rate

T = Absolute junction temperature (K)

Tr = Reference temperature (K)

E_A = Activation energy (eV)

k = Boltzmann's constant: 8.616×10^{-5} (eV/K)

Equation 1 is plotted for a reference temperature of 100°C and activation energies of 0.4 eV to 1.0 eV in Figure 4-24. According to this figure, a 25°C increase in operating temperature above the reference temperature results in approximately a five- to six-fold increase in failure rate with activation energy of 0.6 eV to 0.8 eV. Thus, tight control of package temperature is essential to product reliability.

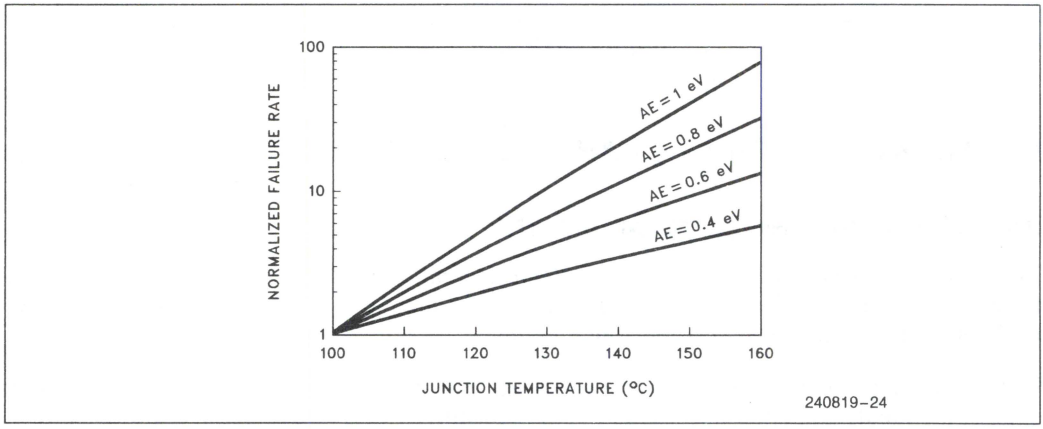


Figure 4-24. Component Failure Rate as a Function of Junction Temperature

Thermal Impedance

The junction-to-ambient and junction-to-case thermal resistance values are used as measures of IC package thermal performance. These parameters are defined by the following relations:

$$\theta_{ja} = \frac{T_j - T_a}{P} \quad (2)$$

$$\theta_{jc} = \frac{T_j - T_c}{P} \quad (3)$$

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \quad (4)$$

where:

θ_{ja} = Junction-to-ambient thermal resistance (C/W)
θ_{jc} = Junction-to-case thermal resistance (C/W)
θ_{ca} = Case-to-ambient thermal resistance (C/W)
T_j = Average die temperature (C)
T_c = Case temperature at a predefined location (C)
P = Device power dissipation (W)
T_a = Ambient temperature

θ_{jc} is a measure of package internal thermal resistance from silicon die to package exterior. This value is strongly dependent upon packaging material, thermal conductivities, and package geometry. On the other hand, θ_{ja} values include not only package internal thermal resistance, but also the conductive and convective thermal resistance from package exterior to the ambient. θ_{ja} values depend on material thermal conductivities and package geometry as well as ambient conditions such as flow rates and coolant physical properties.

To guarantee component functionality and long-term reliability, the maximum device operating temperature is bounded by setting constraints on either ambient temperature or package exterior temperature at predefined locations. Ambient temperature is most often measured at an undisturbed location at a certain distance away from the package. As defined in Intel experiments, the case temperature is measured at the center of the package's top surface. Depending on the ambient and board temperatures in the systems environment, thermal enhancements such as heat fins or forced air cooling may be necessary to meet the case or ambient temperature requirements.

Test Methodology

To calculate thermal resistance values, junction temperature is measured using the temperature-sensitive parameter (TSP) method. This method uses special test structures cut to the same size as the actual device, consisting of resistors and diodes. Resistors are used to simulate the device power dissipation and thus heat up the package. Diodes located at different points on the chip surface are used to measure the temperature.

A single package is mounted either directly or via a socket to a thermal test board, which is oriented vertically in the test chamber. Two different test board designs are used for surface mount and through-hole mount packages, as shown in Figure 4-25. The test chamber volume

is 1 ft.^{3}, and the ambient temperature is measured 12 in. away from the package (see Figure 4-26). Initially, the diodes are forward-biased to a 100 μA constant current source, and the test board assembly is immersed in a constant temperature dielectric fluid bath. By changing the bath temperature, diode voltage output is calibrated versus bath temperature.

Next, the test structure is powered up, and diode voltage drop is monitored until no change is detected in the voltage level, indicating an equilibrium state. At this stage, the diode voltage drop, ambient and case temperatures, and device voltage drop and current are recorded. In moving-air thermal resistance measurements, the test board assembly is exposed to a developed air flow. In this case, air velocity is measured upstream 12 in. away from the board's leading edge, using a hot wire anemometer. Air temperature is also measured at the same point.

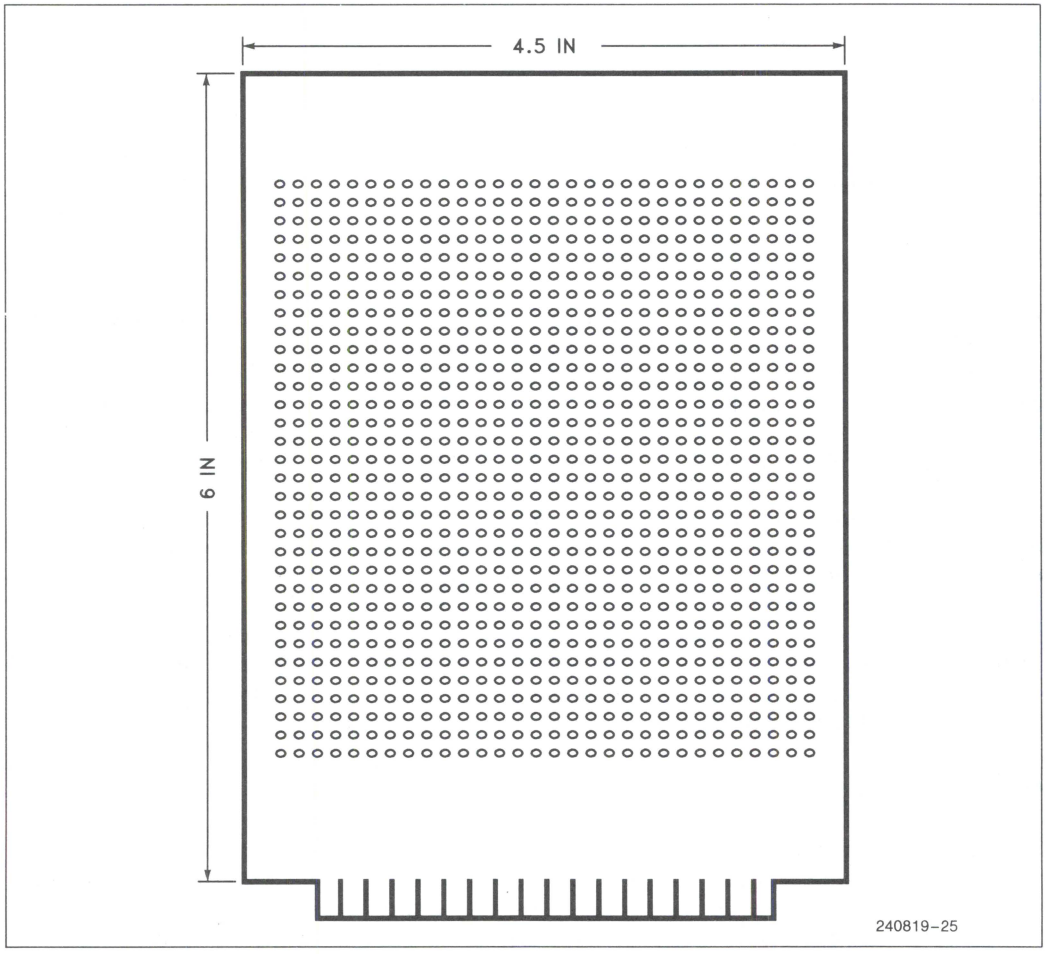


Figure 4-25a. Thermal Test Board for Through Hole Mount Component

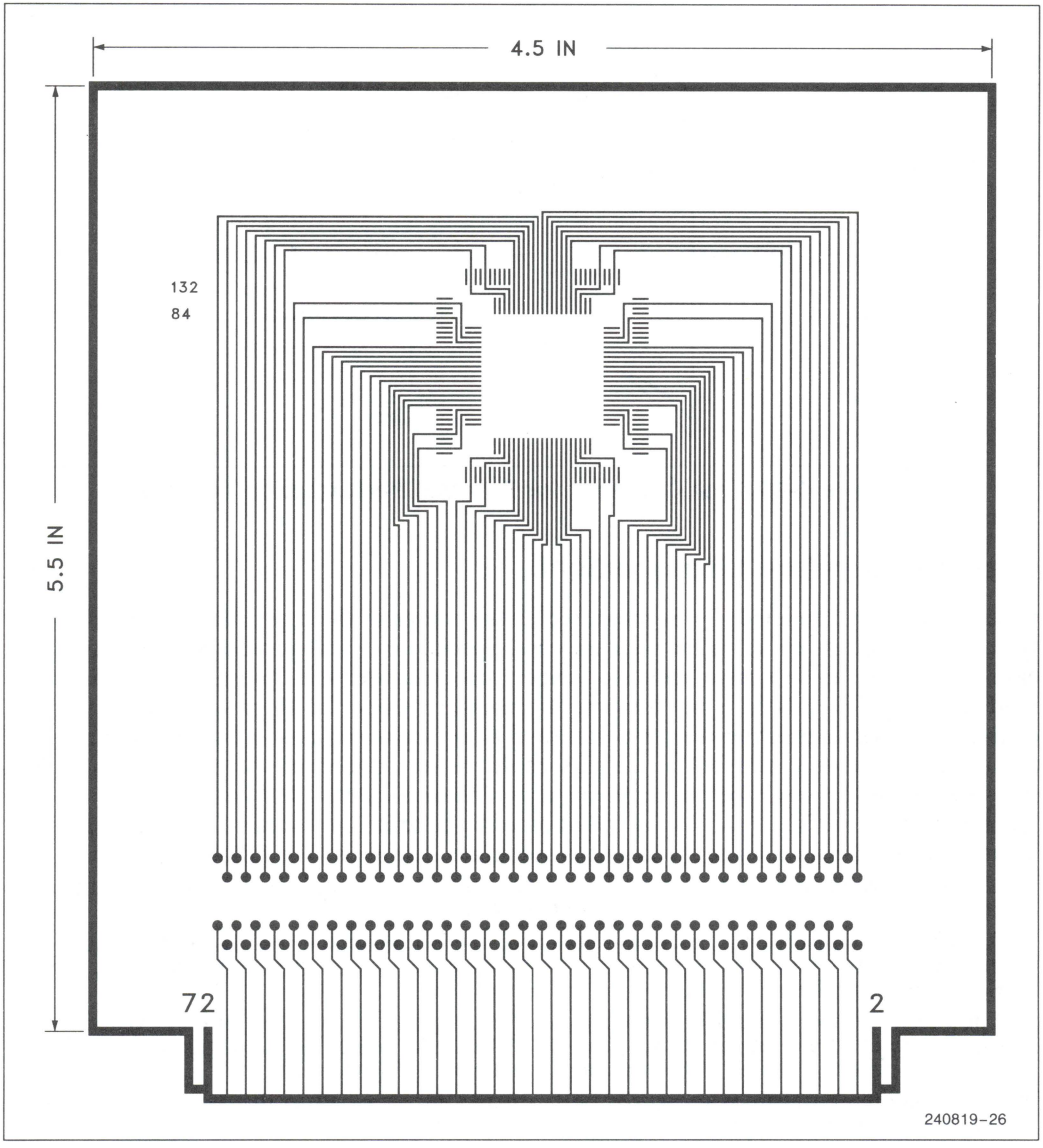


Figure 4-25b. Thermal Test Board for Surface Mount Component

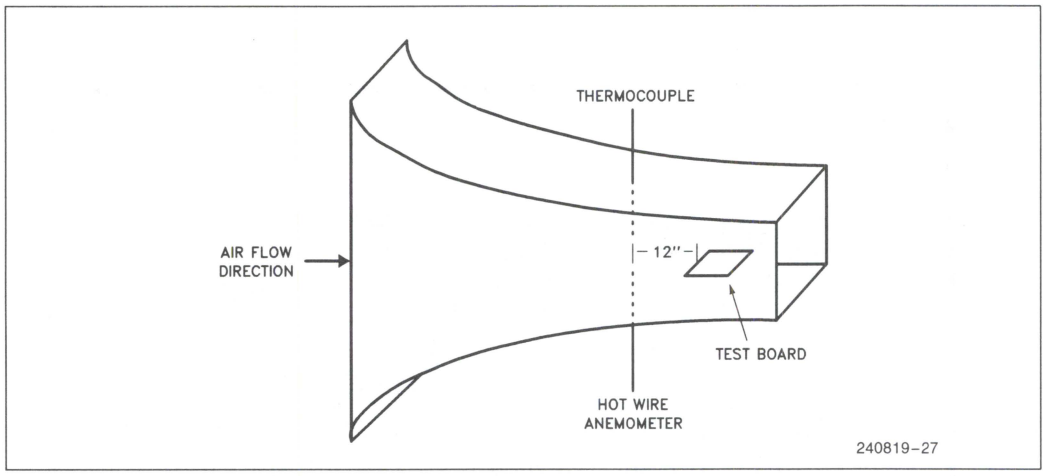


Figure 4-26. Test Chamber for Thermal Performance Testing

Case Temperature Measurement

Case temperature, denoted T_C, is measured at the center of the top surface of the package, typically the hottest point on the package case. Special care is required when measuring the case temperature to ensure an accurate temperature measurement. Thermocouples are often used to measure T_C. Before any temperature measurements, the thermocouples have to be calibrated. When measuring the temperature of a surface which is at a different temperature from the surrounding ambient air, errors could be introduced in the measurements. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface, heat loss by radiation or by conduction through thermocouple leads. To minimize the measurement errors, it is recommended to use the following approach:

- Use 36 gauge of finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number: OB-100)
- The thermocouple should be attached at a 90° angle as shown in Figure 1. When a heat sink is attached a hole (no larger than 0.15″) should be drilled through the heat sink to allow probing the center of the package as shown in Figure 4.27.
- If the case temperature is measured with a heat sink attached to the package, drill a hole through the heat sink to route the thermocouple wire out.

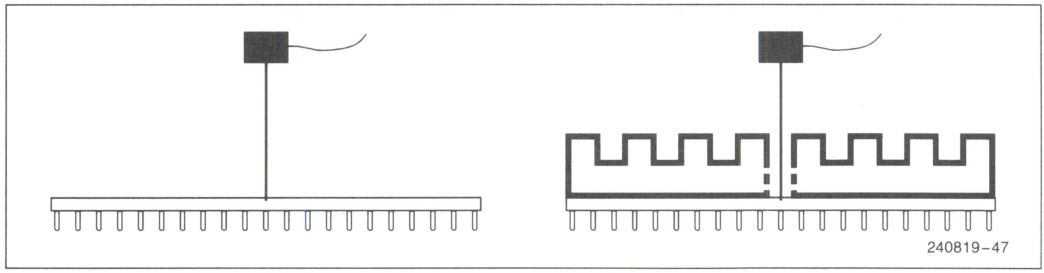


Figure 4-27. Location of Package Case Temperature Measurement

Heat Transfer Modes

To understand the thermal characteristics of ICs, it is necessary to briefly review the processes by which heat is transferred from one point to another. There are three heat transfer modes: conduction, convection, and radiation.

CONDUCTION

Conduction is a process by which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid, or gaseous) or mediums in direct physical contact. In conductive heat flow, the energy is transmitted by direct molecular communication without appreciable displacement of the molecules.

In a one-dimensional system (see Figure 4-28), conductive heat transfer is governed by the following relation:

$$q = -kA\frac{\Delta T}{L} \tag{5}$$

where:

q = Heat flow rate (W)

k = Material thermal conductivity (W/mC)

A = Cross-sectional area (m^2)

$\frac{\Delta T}{L}$ = Temperature gradient (C/m)

Equation 5 indicates that in conduction, the heat flow rate is directly proportional to material thermal conductivity, temperature gradient, and cross-sectional area. Equation 5 can be written as:

$$q = \frac{\Delta T}{L/kA} \tag{6}$$

Using an electrical analogy, if q and ΔT are analogous to current and voltage respectively, L/kA will be analogous to thermal resistance. According to Equation 6, thermal resistance can be expressed in terms of material thermal conductivity and geometrical parameters.

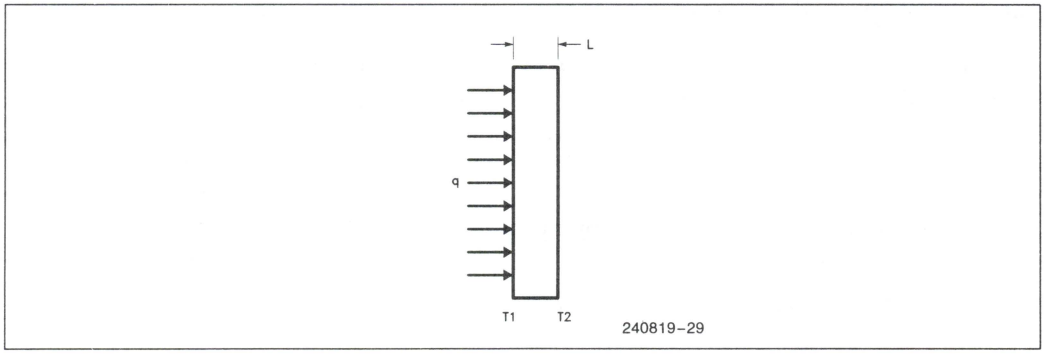


Figure 4-28. One-Dimensional Heat Flow by Conduction

CONVECTION

Convection is a process of energy transport by the combined action of heat conduction, energy storage, and mixing motion. Convection is most important as the mechanism of energy transfer between a solid surface and a fluid. The basic relation that describes heat transfer by convection from a surface presumes a linear dependence on surface temperature rise, and is referred to as Newtonian cooling:

$$q_c = h_c A (T_s - T_a) \tag{7}$$

where:

q_c = Convective heat flow rate from a surface to ambient (W)
A = Surface area (m^2)
T_s = Surface temperature (C)
T_a = Ambient temperature (C)
h_c = Average convective heat transfer coefficient (W/m^2C)

Equation 7 can also be written as:

$$q_c = \frac{T_s - T_a}{1/h_c A} \tag{8}$$

which shows that convective thermal resistance is defined as $1/h_c A$.

In forced convection, fluid flow is caused by an external factor such as a fan, while in free or natural convection, fluid motion is induced by density differences resulting from temperature gradients in the fluid. Under the influence of gravity or other body forces, these density differences give rise to buoyancy forces that circulate the affected fluid and convect heat toward or away from surfaces wetted by the fluid.

RADIATION

Thermal radiation is defined as radiant energy emitted by a medium by virtue of its temperature, without the aid of any intervening medium. The physical mechanism of radiation is not yet completely understood. Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons. Neither viewpoint completely describes the nature of all observed phenomena.

The amount of heat transferred by radiation between two bodies at temperatures T1 and T2 is governed by the following expression:

$$q = \epsilon \sigma A (T_1^4 - T_2^4) \tag{9}$$

where:

q = Amount of heat transferred by radiation (W)
ϵ = Emissivity $0 < \epsilon < 1$
σ = Stefan-Boltzmann constant, 5.67×10^{-8} ($W/m^2 K^4$)

A = Area (m^2)

F_{12} = Shape factor between surfaces 1 and 2 (A fraction of surface 1 radiation seen by surface 2)

T_1, T_2 = Surface temperatures (K)

For radiation to make a rather significant contribution compared to either natural convection or forced convection mechanisms, a relatively large temperature difference must exist between T_1 and T_2. In the case of most low-power electronic applications, these temperature differences are relatively small, and therefore, radiation effects are normally neglected. But for power applications, heat transfer by radiation should be considered. To compare radiative and convective effects, a radiation heat transfer coefficient is defined as:

$$h_r = \epsilon \sigma F_{12} (T_1^2 + T_2^2) (T_1 + T_2) \quad (10)$$

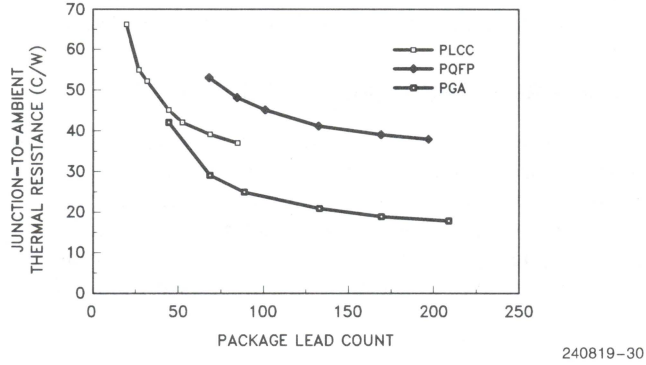
where h_r is the radiative heat transfer coefficient.

Factors Impacting Package Thermal Resistance

The thermal resistance of a package is not a constant entity. There are several packaging and environmental parameters as well as mounting configurations that impact thermal resistance values. The following is a summary of those parameters.

PACKAGE SIZE

As shown by the one-dimensional conductive and convective thermal resistance expressions (see Equations 6 and 8), thermal resistance is inversely proportional to area. This means that as the packages get larger, thermal resistance becomes smaller due to an increase in the heat transfer area. Figure 4-29 shows typical junction-to-ambient thermal resistance values as a function of lead count for different package families. According to this figure, thermal resistance is lower for higher lead counts (larger package size) of the same package family.



NOTE:
Pin Grid and Plastic Surface Mount Packages.

Figure 4-29a. Effect of Package Size on Thermal Resistance of PLCC, PQFP, and PGA Packages

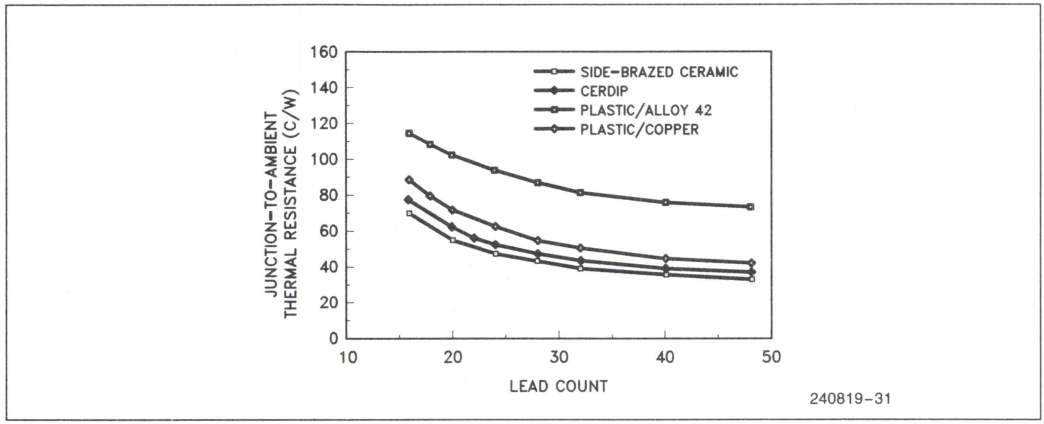


Figure 4-29b. Effect of Package Size on Thermal Resistance of Plastic and Ceramic Dual-In-Line Packages

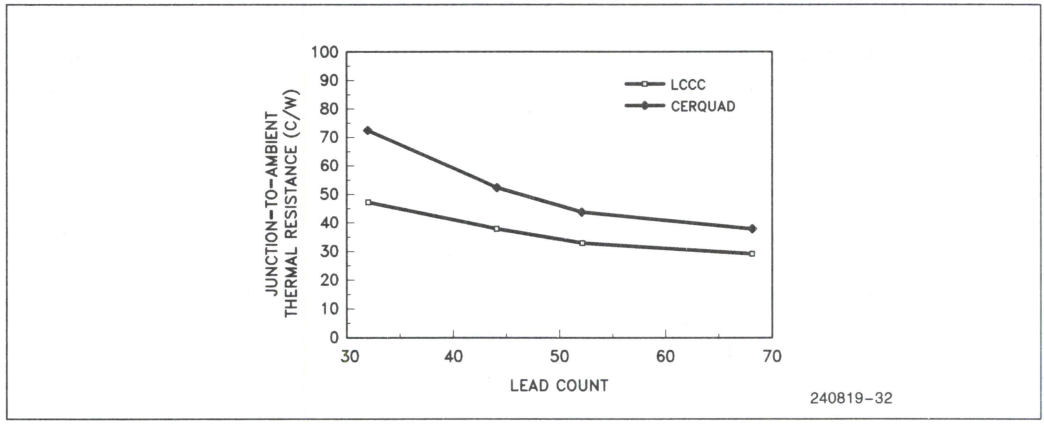


Figure 4-29c. Effect of Package Size on Thermal Resistance of CerQuad and Leadless Ceramic Chip Carriers

PACKAGING MATERIAL THERMAL CONDUCTIVITY

Again, the one-dimensional conductive thermal resistance expression shows that thermal resistance is inversely proportional to the thermal conductivity of the packaging material. For example, aluminum oxide, the most commonly used ceramic material, has a thermal conductivity that is an order of magnitude larger than plastic materials. As a result, the internal resistance of ceramic packages is substantially lower than the plastic packages from the same family, resulting in lower overall thermal resistance (see Figure 4-30, CQFP vs. PQFP).

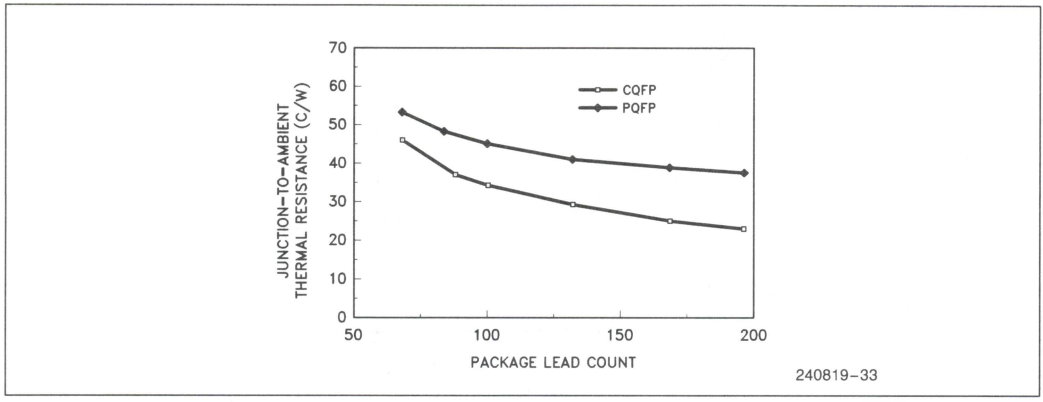


Figure 4-30. Effect of Packaging Material on Thermal Resistance

DIE SIZE

As shown in Figure 4-31, thermal resistance reduces as the die size increases. Increase in die size results in lower power density and larger effective heat transfer area. The changes in thermal resistance are sharper at smaller die sizes, and as the die size approaches package size, they become less significant, raised to the power n, n = 0.25 for laminar flow, n = 0.33 for turbulent flow.

4

DEVICE POWER DISSIPATION

An increase in device power, which will raise the temperature of the package, results in lower junction-to-ambient thermal resistance (θ_{ja}) values in natural convection, while not affecting θ_{ja} in forced convection. The values of θ_{jc} do not change significantly as a function of the device power both in natural and forced convection (see Figure 4-32). In natural convection, the convective heat transfer coefficient is proportional to the temperature difference between the case and the ambient, raised to the power n, n = 0.25 for laminar flow, n = 0.33 for turbulent flow. Therefore, the case-to-ambient thermal resistance will be inversely proportional to this temperature, temperature difference raised to the power n, and as a result, to the device power.

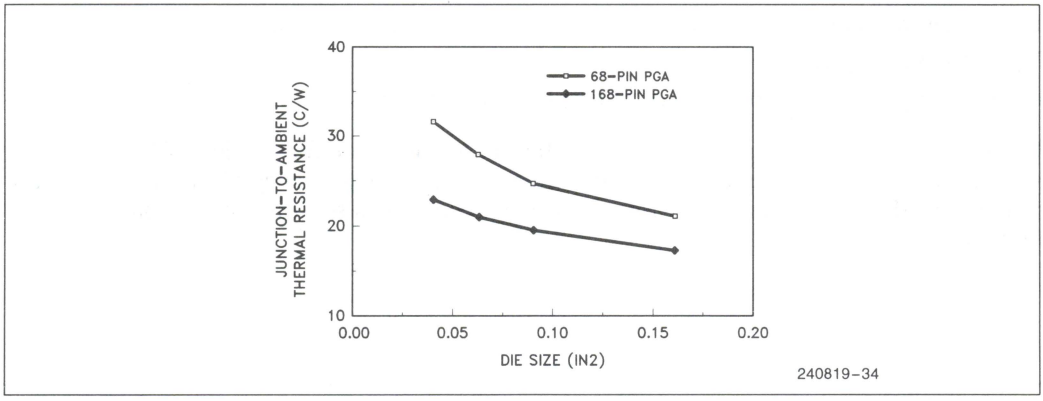


Figure 4-31. Effect of Die Size on Package Thermal Resistance

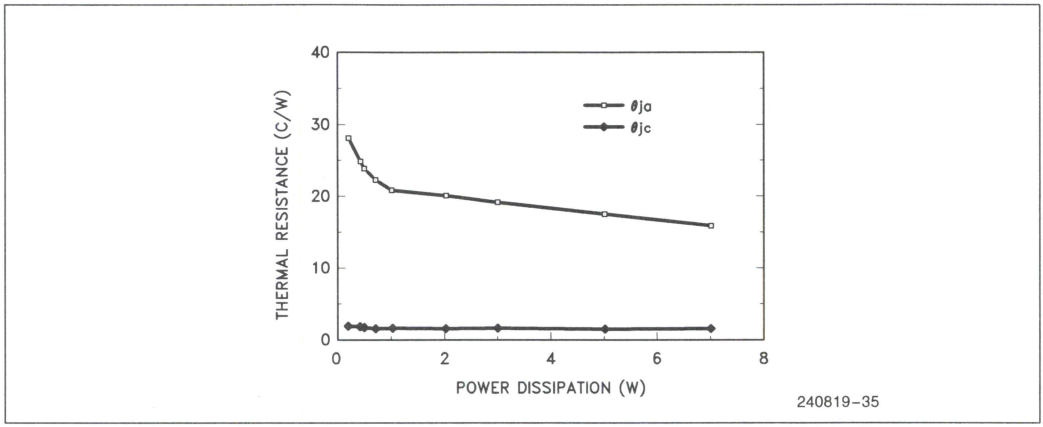


Figure 4-32. Effect of Power Dissipation on Thermal Resistance

It should be noted that the error in θ_{ja} also increases at lower power levels, because both temperature and power measurements are less accurate.

In the case of forced convection, the heat transfer coefficient does not depend on temperature explicitly. Dependency on temperature is only due to changes in material properties. These properties do not vary significantly for air within the temperature ranges normally encountered. However, at low flow rates, natural and forced convection may have effects that are of the same order of magnitude (mixed convection). In this region, a small dependency on power may be observed, but as the flow rate increases, power dependency disappears.

AIR FLOW RATE

In forced convection, case-to-ambient thermal resistance is a function of the air flow rate, as shown by Equation 11:

$$\theta_{ca} = K/V^m \qquad (11)$$

$$\theta_{ja} = \theta_{jc} + K/V^m$$

where:

K = Constant depending on air properties as well as package geometry

V = Air velocity (m/s)

m = $\frac{1}{2}$ and $\frac{4}{5}$ for laminar and turbulent flow respectively

Figure 4-33 shows how θ_{ja} varies as a function of air flow rate for 168-lead PGA with and without heat fins. At lower air flow rates, there is a strong dependency of θ_{ja} on the air flow rate, but as the air flow rate increases, θ_{ja} values become less sensitive to the changes in the flow rate.

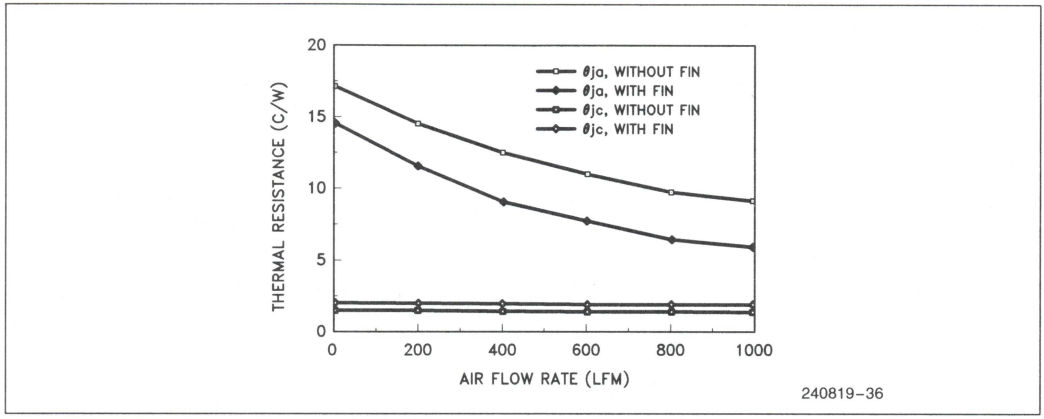


Figure 4-33. Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package

Mounting Parameters

PC BOARD SIZE AND THERMAL CONDUCTIVITY

Figure 4-34 shows that a printed circuit board can act as a heat fin, resulting in lower junction-to-ambient thermal resistance due to the increased heat transfer area. The effect of the board size on overall thermal resistance may vary, depending on the thermal resistance between the junction and the board compared to the resistance between the case and the ambient. Smaller packages with a relatively high case-to-ambient thermal resistance value are more dependent on the board for transfer of heat to ambient than are the larger size packages.

Another factor that impacts the thermal resistance from board to ambient is board thermal conductivity. As board thermal conductivity or board thickness increases, the spreading resistance through the board reduces, and a larger board area becomes available for heat transfer to the ambient.

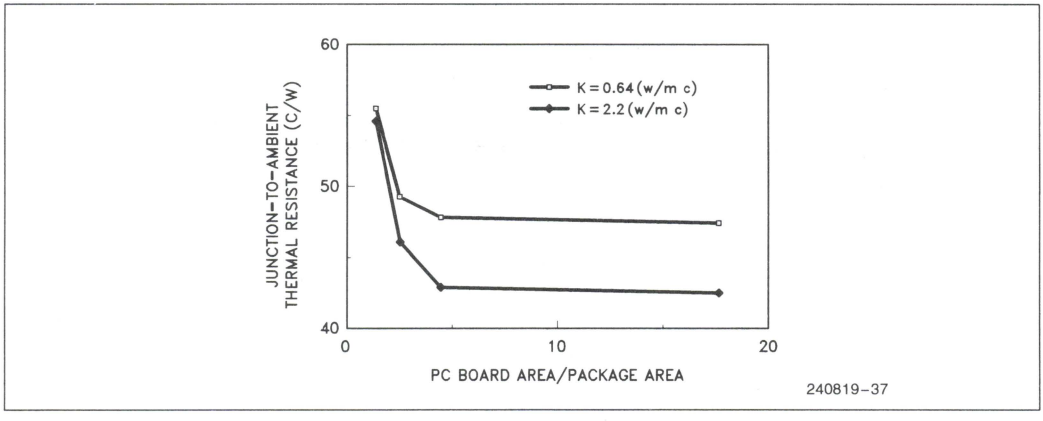


Figure 4-34. Effect of PC Board Material and Size on Thermal Resistance of 132-Lead PQFP

PC BOARD TEMPERATURE

PC board temperature is an important parameter that impacts package thermal resistance and is normally ignored. For a board of specific size and properties with only the component under consideration mounted on it, there is a unique equilibrium temperature distribution (T_b) on the board under fixed environmental and mounting conditions. However, if there are other components on the board or the board is attached to a heat sink, the value of T_b may increase or decrease. A change in board temperature will also change junction temperature and consequently junction-to-ambient thermal resistance. This value of junction-to-ambient thermal resistance, which is different from the value measured when the board is not influenced by other heating or cooling factors (θ_{ja}), is referred to as apparent thermal resistance or systems-level thermal resistance ($\theta_{ja,s}$).

In almost all practical applications, PC boards are populated by many components, and heating of one package influences other packages. In order to get a relatively good estimate of system thermal resistance ($\theta_{ja,s}$), and as a result, of junction temperature, $\theta_{ja,s}$ and θ_{ja} values must be correlated through another parameter. As it turns out, this parameter is T_b, and by breaking up the package thermal resistance into a simple resistor network, a relation can be derived between $\theta_{ja,s}$, θ_{ja}, and T_b. Therefore, by using the correlation θ_{ja}, and by measuring T_b, junction temperature can be calculated.

Figure 4-35 shows a simple equivalent single-resistor network for any package. In this model, it is assumed that the heat path is from junction to package boundary, and from there, a portion of the heat is transferred directly to the ambient, while the rest goes to the board and is distributed and transferred to the ambient.

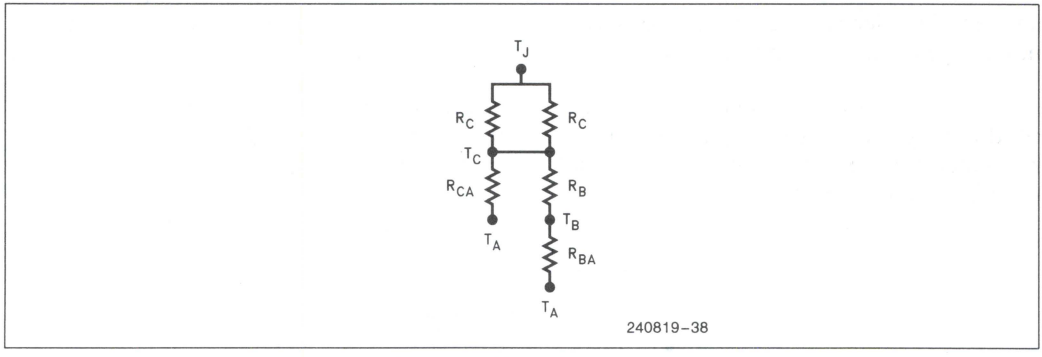


Figure 4-35. Simplified Resistor Network

It should be noted that the model shown in Figure 4-35 is simplified, and the actual package resistor network model can be more complex. The following expression shows the relation between $\theta_{ja,s}$ and θ_{ja} and board temperature rise ($T_b - T_a$):

$$\theta_{ja,s} = \theta_{ja} + S\left(\frac{T_b - T_a}{P}\right) - \frac{S\,R_a\,R_{ba}}{(R_a + R_b + R_{ba})}$$

$$S = \frac{R_a}{R_a + R_b} \qquad (12)$$

where:

P = Power dissipation (W)
R_a = Case-to-ambient resistance (C/W)
R_b = Case-to-board resistance (C/W)
R_{ba} = Board-to-ambient resistance (C/W)
R_c = Junction-to-case resistance (C/W)
S = Sensitivity parameter, $R_a/(R_a + R_b)$ $(0 < s < 1)$
$T_b - T_a$ = Board temperature rise over ambient (C)

Equation 12 shows a linear dependence of $\theta_{ja,s}$ on board temperature rise; as the board temperature increases or decreases, the system thermal resistance will increase or decrease. The rate of these changes is dictated by sensitivity parameter s, which in turn depends on R_a/R_b. As R_a/R_b increases, thermal resistance becomes more sensitive to board temperature rise; in other words, the package becomes more thermally coupled with other components on the board. Large values of R_a/R_b indicate that the package depends more on the board for transfer of heat to the ambient than on direct heat transfer to the ambient (larger packages vs. smaller packages). On the other hand, as R_a/R_b decreases, s decreases. Smaller R_a/R_b means a higher degree of insulation between the package and the board. For example, the thermal resistance of a package with a copper lead frame is more sensitive to board temperature rise than its counterpart with an Alloy 42 lead frame, as shown in Figure 4-36.

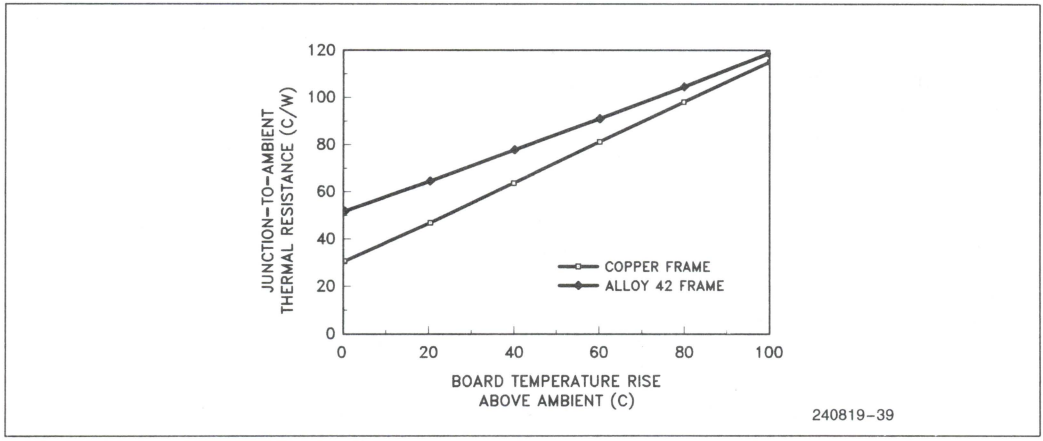


Figure 4-36. Effect of Board Temperature Rise on Thermal Resistance of 132-Lead PQFP with Copper and Alloy 42-Lead Frames

To determine sensitivity factor s and intercept in expression 12, the package system thermal resistance can be measured under two different board temperature conditions (θ_{ja} is assumed to be known).

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REVISION SUMMARY

The main differences between 240819-003 rev and the -002 version are the following:

- Revised PGA, MM, PQFP and PLCC Electrical Data
- Added QFP, SQFP and TQFP Electrical Data
- Added section: case temperature measurement

Physical Constants of IC Package Materials

5

CHAPTER 5
PHYSICAL CONSTANTS OF IC PACKAGE MATERIALS

The following tables list the typical physical properties of materials used in IC packages.

Table 5-1. Case Material Characteristics

Properties		Units	Alumina	Kovar	Molding Compound	Sealing Glass
Specific Gravity			3.6–3.7	8.4	1.79–1.85	4.7
Mechanical Properties	Modulus of Elasticity	GN/m^2	255	138	$E_1 = 11.7$ $E_2 = 0.1$	5.7
	Tensile Strength	MN/m^2	157	627	19.98	
Thermal Properties	Thermal Conductivity (20°C)	W/m/ °C	18–19.6	17.5	0.58–0.67	0.6
	Coefficient of Thermal Expansion (40–250°C)	10^{-6}/°C	7.0–7.2	5.3	$\alpha_1 \leq 23$ $\alpha_2 \leq 80$	6.3–7.0
Electrical Properties	Electrical Resistivity	Ω . cm	10^{14}	49×10^{-6}	5×10^{12}	$>10^{11}$
	Dielectric Constant (1 MHz)		7.9–10.0		≤5.0	11.5
Flammability Rating		Inch			1/8"	

Table 5-2. Lead/Lead Frame Material Characteristics

Properties		Units	Copper Alloy MF 202	Alloy 42	Kovar	TAMAC5	Olin194
Specific Gravity			8.88	8.1	8.4	8.9	8.8
Mechanical Properties	Modulus of Elasticity	GN/m^2	113	145	138	123	121
	Tensile Strength	MN/m^2	490–590	588–735	627	450–510	480–519
Thermal Properties	Thermal Conductivity (20°C)	W/m/ °C	160	15.7	17.5	190	263
	Coefficient of Thermal Expansion	10^{-6}/°C	17.0	4.5	5.3	16.7	16.3
Electrical Properties	Electrical Resistivity	Ω . cm	5.7×10^{-6}	57×10^{-6}	49×10^{-6}	3.5×10^{-6}	2.6×10^{-6}

Table 5-3. Soldering Material Characteristics

Property	Tin-Lead Plating	Tin-Lead Eutectic Solder	Tin	Gold	Copper/Silver Braze
Melting Point (°C)	200–225	~ 183	232	1063	850

Table 5-4. Die Attach Material Characteristics

Property	Mechanical Properties			Thermal Properties		Electrical Properties		Flammability Rating
	Specific Gravity	Modulus of Elasticity	Tensile Strength	Thermal Conductivity	Coefficient of Thermal Expansion	Electric Resistivity	Dielectric Constant (1 MHz)	
Silver Filled Glass	4.5		$>1.0 MN/m^2$	270 W/M/K	$8 \times 10^{-6/°C}$	1.2×10^{-5} Ω . cm		N/A

REVISION SUMMARY

The main difference between 240820-003 revision and the -002 version is as follows:

- Added Die Attach Charactertistics
- Deleted Quartz Glass
- Added TAMAC5 and Olin194
- ESD/EOS Precautions (Literature Order Number 241422-001)

Component Handling Precautions

6

CHAPTER 6
COMPONENT HANDLING PRECAUTIONS

ESD

Electrostatic Discharge (ESD)

Electrostatic discharge (ESD) costs the electronics industry millions of dollars each year in damaged components, non-functional circuit boards, and scrambled or missing information. ESD can occur in the manufacturing, shipping, receiving, and field handling of integrated circuits or computer boards with no visible signs of damage. A malfunction in these components or boards can occur immediately or the apparatus may perform for weeks, months, or even years before an unpredictable and premature breakdown causes a field failure.

Why Should I Care About Electrostatic Discharge?

If you incorporate electronic components or boards into your products, ESD damage can have a direct impact on your company's reputation and profits. That's because electrostatic damage directly affects the quality and reliability of your products. However, for a small investment in time, manpower, and equipment, you can virtually eliminate ESD-caused problems. The tangible benefits to you include:

- Higher manufacturing yields
- Less rework and inventory
- Reduced overall costs
- Fewer field failures and warranty calls
- Increased product reliability
- More repeat business resulting in greater profits

Intel's Commitment to Stamp Out ESD Damage

Because Intel makes and uses electronic components, it has implemented a comprehensive ESD prevention program to ensure that its products are delivered to customers with the highest possible reliability. Our experts would like to share with our suppliers and customers what they have learned about ESD control. Using this information, you can implement similar preventive practices in your factories and warehouses. As a result, all of us can then assure that our products remain free of hidden component failures.

What is ESD?

Technically, ESD is the transfer of electrical charge between two bodies at different potentials, either through direct contact or through an induced electrical field. It is the phenomenon that gives you a mild shock when you walk across a carpeted floor and then touch a doorknob. While this discharge gives a harmless shock to humans, it is lethal to sensitive electronics. For example, the simple act of walking across a vinyl floor can generate up to 12,000V of static electricity. That is many times the charge needed to ruin a standard Shottky TTL component.

November 1993
Order Number: 241422-002

There are several technical failure mechanisms associated with ESD damage to microelectronic devices. These failure mechanisms can include gate oxide breakdown, junction spiking, and latch-up.

Gate oxide failures are a breakdown of the dielectric between the transistor gate and channel resulting in excessive leakage or a functional failure.

Junction spiking failures are a migration of the metallization through the source/drain junction of MOS transistors causing leakage or a functional failure.

Latch-up failures can be triggered by ESD, causing an internal feedback mechanism that gives rise to temporary or permanent loss of circuit function.

Common Causes of ESD

Electrostatic generation arising from friction between two materials is called triboelectric charging. It occurs when two materials are separated or rubbed together. Examples include:

- Opening common plastic bag
- Removing adhesive tape from a roll or container
- Walking across a floor
- Transporting computer boards or components around in their trays on carts
- Sliding circuit boards on a work bench

When handling parts or their containers, ungrounded personnel can transfer high static charges. Unless these static charges are slowly dissipated, the ESD event will inflict damage.

Electrical fields are able to penetrate electrical devices. An ungrounded person handling a component or computer board in a non-static shielding container can cause a large charge to be transferred through the container into the sensitive electronic device.

ESD Occurs at All Levels of Integration

Electrostatic discharge is not selective when damaging your products. It can strike components directly or indirectly by passing to the component via connectors and cables. Components mounted on circuit boards are also susceptible.

In-line film resistors between inputs and off-board connectors provide only marginal ESD protection and are often damaged themselves.

What Can I Do To Prevent ESD?

Fortunately, preventing ESD is relatively easy and inexpensive. The two areas of focus are 1) eliminating static charges from the work place, and 2) properly shielding components and assemblies from static fields.

Eliminating static electricity in the work place is accomplished by grounding operators, equipment, and parts (components and computer boards). Grounding prevents static charge buildup and electrostatic potential differences. Electrical field damage is averted by transporting products in special electrostatic shielding packages.

There are many vendors of ESD-protective equipment who are willing to audit your facilities, recommend appropriate procedures and materials, and assist in their implementation. You should consult with such a firm to determine your exact requirements; however, the basic components of a sound ESD prevention program are listed below.

An Effective Work Place Should Be Outfitted with the Following Items:

ESD protective clothing/smocks. Street clothing must not come in contact with components or computer boards since the various materials in clothing can generate high static charges. ESD protective smocks, manufactured with conductive fibers, are recommended.

Electrostatic shielding containers or totes. These containers (bags, boxes, etc.) are made of specially formulated materials which protect sensitive devices during transport and storage.

Antistatic or dissipative carriers. These provide ESD protection during component movement in the manufacturing process. It must be noted that antistatic materials alone will not provide complete protection. They must be used in conjunction with other methods such as totes or electrostatic shielding bags.

Dissipative table mat. The mat should provide a controlled discharge of static voltages and must be grounded. The surface resistance is designed such that sliding a computer board or component across its surface will not generate more than 100V.

Personal grounding. A wrist strap or ESD cuff is kept in constant contact with bare skin and has a cable for attaching it to the ESD ground. The purpose of the wrist strap is to drain off the operator's static charge. The wrist strap cord has a current-limiting resistor for personnel safety. Wrist straps must be tested frequently to assure that they are undamaged and operating correctly. When a wrist strap is impractical, there are special heel straps or shoes which can be used. These items are effective only when used in conjunction with a dissipative floor.

ESD protective floor or mat. The mat must be grounded through a current-limiting resistor. The floor or mat dissipates the static charge of personnel approaching the work bench. Special conductive tile or floor treatment can be used if mats are not practical or cause a safety hazard. Chairs should be conductive or grounded with a drag chain to the flooring.

Summary

Intel uses the full range of electrostatic discharge prevention techniques. We invest in proper employee training, purchase appropriate ESD protection equipment and supplies and adapt our handling and manufacturing procedures for ESD prevention requirements. The same attention to detail is required of all our suppliers, factories, repair centers, and field service staff.

Intel is committed to helping its partners—both suppliers and customers—to manage the ESD problem. If we can be of further assistance in your efforts to eliminate electrostatic discharge damage, please contact the Intel Components Quality Question Line:
USA 1-800-852-2040, Canada 1-800-845-5841, or your local Intel Sales Office.

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EOS

Electrical Overstress (EOS)

EOS is the number one cause of damage to IC components. This section describes EOS and how to prevent it.

How EOS Damages a Component

Damage is caused by thermal overstress to a component's circuitry. The amount of damage caused by EOS depends on the magnitude and duration of electrical transient pulse widths. We can broadly classify the duration of pulse widths into long (>100 μs) and short (<100 μs) types, and magnitude into exceeding an individual component's EOS threshold. For short pulse widths the most common failure mode is junction spiking.

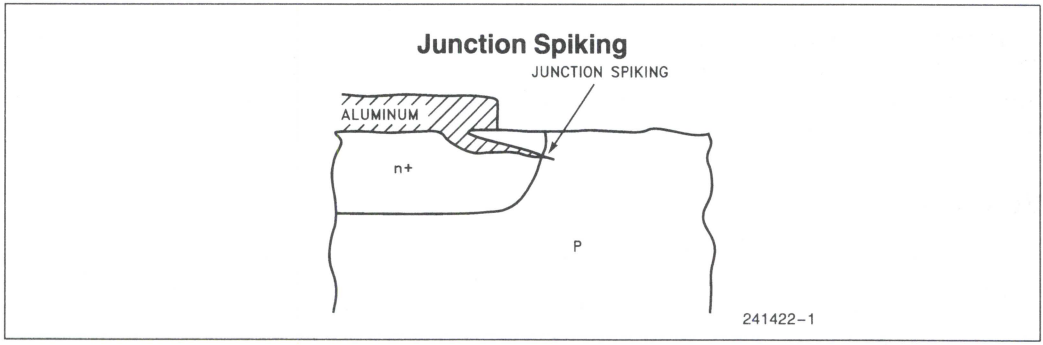

Figure 6-1. Junction Spiking Failure

For long electrical pulse widths the most common failure modes are melted metallization and open bond wires.

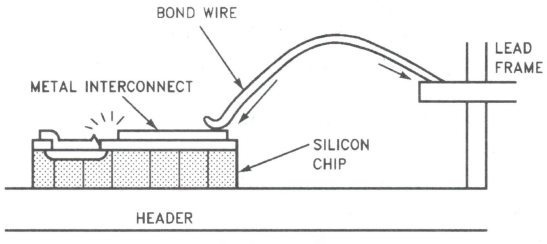

Figure 6-2. Melted Metallization Failure

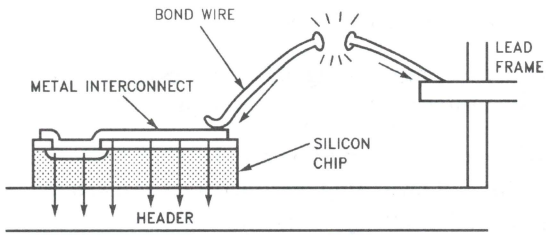

Figure 6-3. Open Bond Wire Failure

Common Causes of EOS

Inadequate work procedures:
— Lack of standard work procedures
— Incorrect device orientation
— Insertion/removal of components with power on
— Boards/units not well connected, then power applied

Noisy Production Environments:
— Lack of power line conditioners
— Lack of A.C. line filters

Improper testing at device or board level can create EOS:
— Hot switching effect
— Incorrect test sequence such as application of signals to Device Under Test (DUT) before powering up chip
— Application of excessive voltages to chip beyond spec limits
— Poorly designed electrical stress tests such as burn-in which overstresses sensitive chips

Use of low quality power supplies:
— Poor design considerations can lead to noise sources especially in switching power supplies
— Lack of power supply overvoltage protection circuits
— Insufficient line filtering and/or transient suppression at the input stage of power supplies
— Incorrect selection of fuse providing inadequate protection

Lack of Proper Equipment and Line Monitoring:
— Equipment not grounded
— Loose connections causing intermittent events
— Poor wire maintenance
— AC supply lines not monitored for voltage transients or noise

Prevention of EOS

Establish and follow proper work procedures.

Conduct regular AC supply line monitoring, and if necessary, install EOS line control equipment such as incoming line filtering and transient suppression circuits.

Ensure proper testing of components and boards:
— Check test programs for hot switching and incorrect test sequence
— Solicit maximum specification ratings from manufacturers to ensure devices are not overstressed
— Ensure reliability stress tests are properly designed, especially during burn-in
— Check for excessive noise levels
— Use transzorbs to clamp voltage spikes

Use quality power supplies with the following features:
— Overvoltage protection
— Proper heat dissipation
— Use of fuses at critical locations

Adhere to a strict equipment maintenance program to ensure:
— Equipment is properly grounded
— There are no loose connections

PGA Insertion

For guideline information regarding PGA insertion, please request a copy of item # 8130 by calling the Intel FAXBACK line U.S. 1 800 628-2283 Europe 44-793-4960646

Revision Summary

Added reference for PGA insertion information.

Surface Mount Technology 7

CHAPTER 7
SURFACE MOUNT TECHNOLOGY

INTRODUCTION

Traditional through-hole methods of assembling conventional electronic assemblies reached their limits in terms of improvements in cost, weight, volume, and reliability at approximately 68L. SMT allows production of more reliable assemblies at increased board density, reduced weight, volume, and cost. As shown in Figure 7-1, the weight of printed board assemblies (PBAs) using SMT is reduced because surface mount components (SMCs) can weigh up to 10 times less than their conventional counterparts and occupy about one-half to one-third the space on the printed board (PB) surface (see Figure 7-2). SMT also provides improved shock and vibration resistance due to the lower mass of components. The smaller lead lengths of surface mount components reduce parasitic losses and provide more effective decoupling (see Figure 7-3). The source for Figures 7-1 through 7-3 is Reference 1.

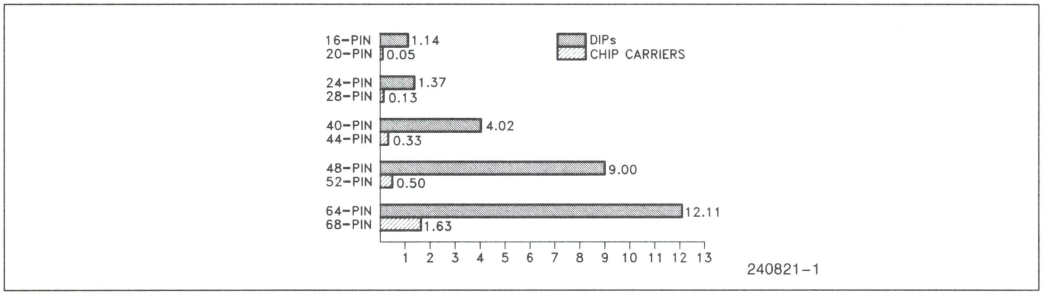

Figure 7-1. The Weight of Various Lead-Count Chip Carriers for SMT Compared to the Weight of an Equivalent DIP

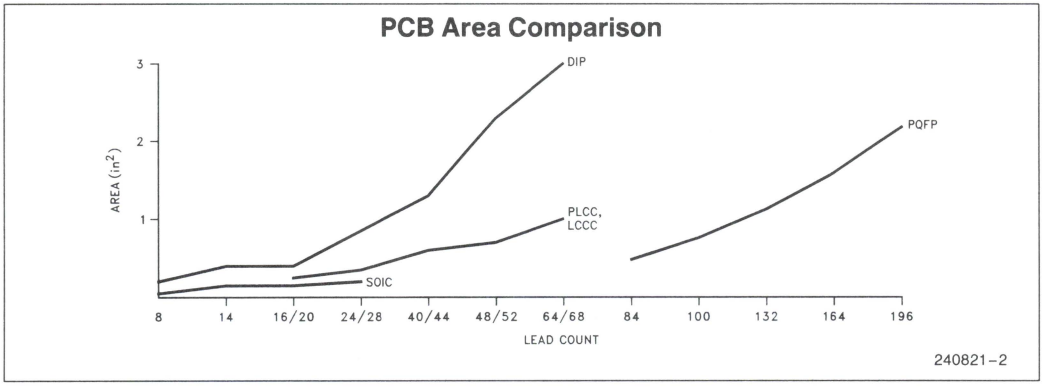

Figure 7-2. Comparison of PCB Level Area with DIP Packaging and SMT Packaging (Leadless Ceramic Chip Carriers, Small Outline Packages, and Plastic Quad Flatpaks). SMT Results in a Significant Reduction on Board Area.

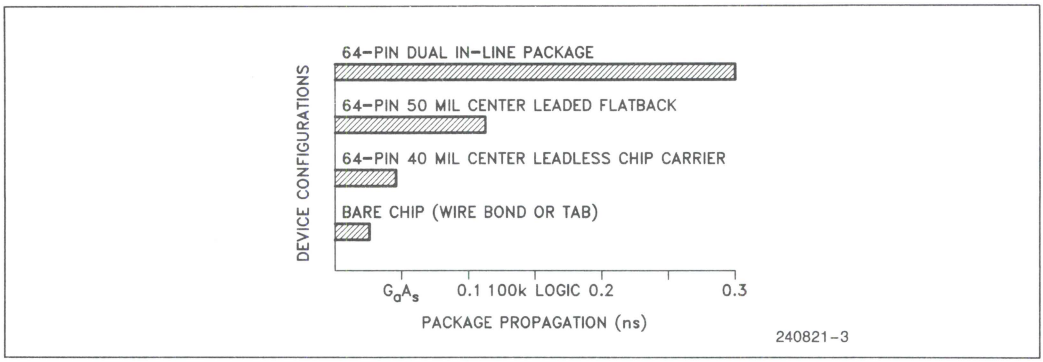

Figure 7-3. Comparison of the Propagation Delays of a Leadless Ceramic Chip Carrier and a DIP

The smaller size of SMCs and the option of mounting them on either or both sides of the PB can reduce board real estate by four times. For example, half a megabyte of 256K DRAM memory with conventional DIP components will require about 4.0 x 4.0 in. of PC board area. The same board with surface mount components attached on a single side can accommodate one megabyte of memory. A cost savings of 30% or better can also be realized through a reduction in material and labor costs associated with automated assembly.

TYPES OF SURFACE MOUNT TECHNOLOGY

SMT replaces through-hole by surface mount components. The assembly is soldered by reflow (vapor phase/infrared/convection) and/or wave soldering processes if there is a mix of surface mount and through-hole mount components. Figure 7-4 shows an example of an active component in surface mount plastic leaded chip carrier configuration (PLCC) and its conventional leaded equivalent. When attached to PBs, both active and passive SMCs form three major types of SMT assemblies, commonly referred to as Type 1, Type II, and Type III (see Figure 7-5).

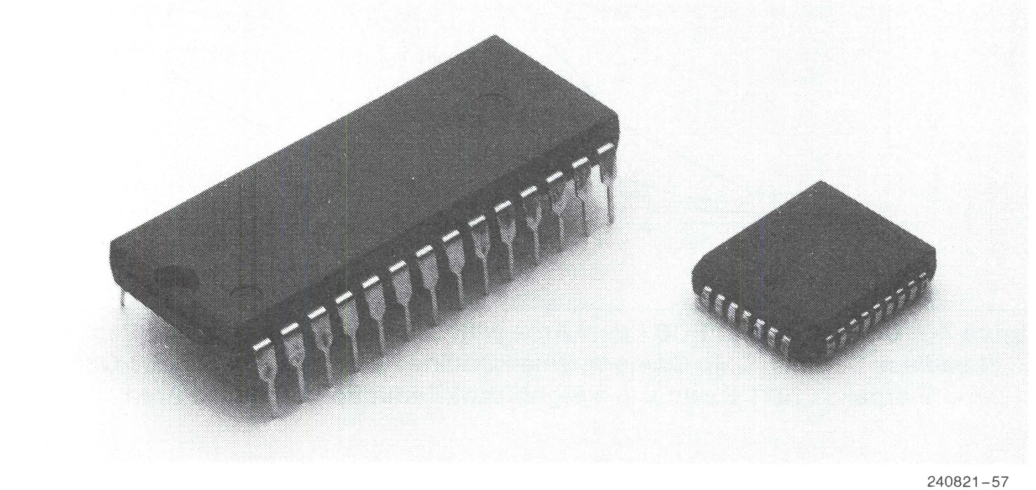

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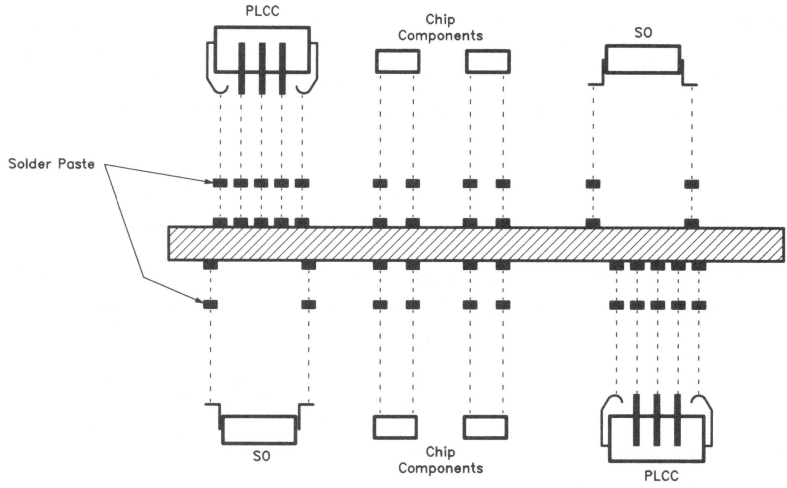
Figure 7-4. Surface Mount Active Components and its Conventional Equivalent

Type I



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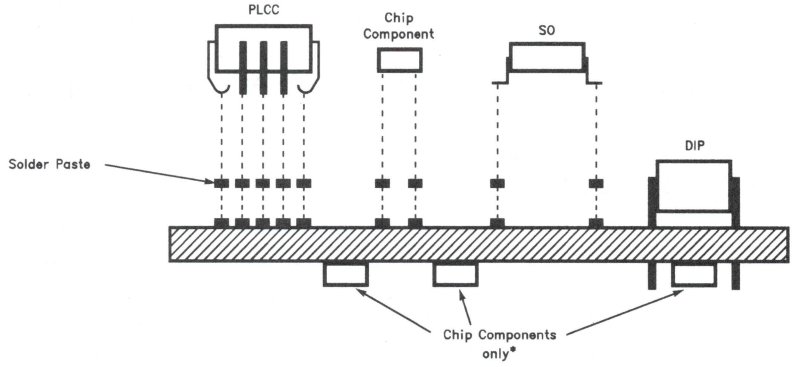
Type II



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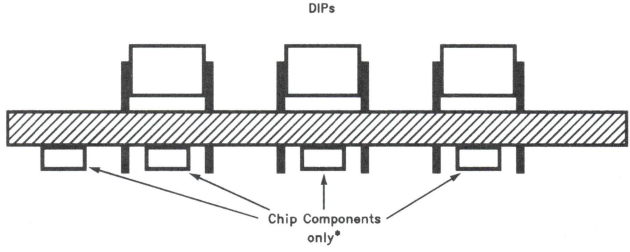
Type III



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NOTE:
Intel does not recommend active devices be immersed in solder wave.

Figure 7-5. Surface Mount Technology Board Types

The process sequence for Type III SMT is shown in Figure 7-6. Leaded components are auto-inserted using existing equipment. The assembly is turned over, and adhesive is applied. Next, passive SMCs are placed by a "pick-and-place" robot, the adhesive is cured, the assembly is turned over, and the wave-soldering process is used to solder both leaded and passive SMCs in a single operation. Finally, the assembly is cleaned, inspected, repaired if necessary, and tested. Note that only passive chip components are surface mounted by exposure to solder wave.

The process sequence for Type I SMT is shown in Figure 7-7. Solder paste is screened on to the board, components are placed, and the assembly is baked to drive off volatiles from the solder paste. Currently, pastes are available that do not require baking. Finally, the assembly is reflow soldered (vapor phase or infrared) and cleaned. For double-sided Type I SMT assemblies, the board is turned over, and the process sequence just described is repeated.

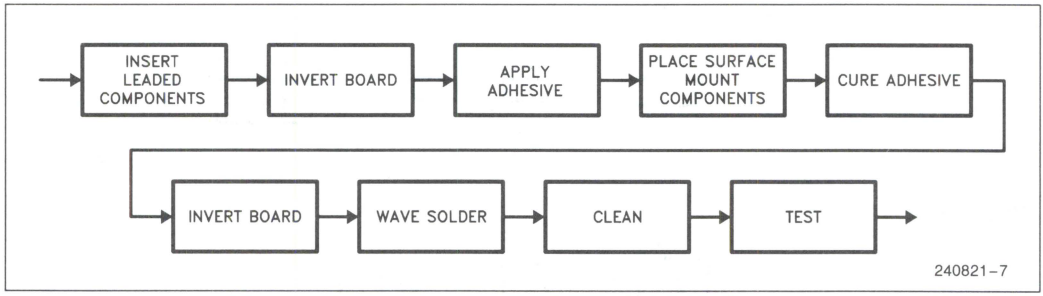


Figure 7-6. Typical Process Flow for Underside Attachment (Type III SMT)

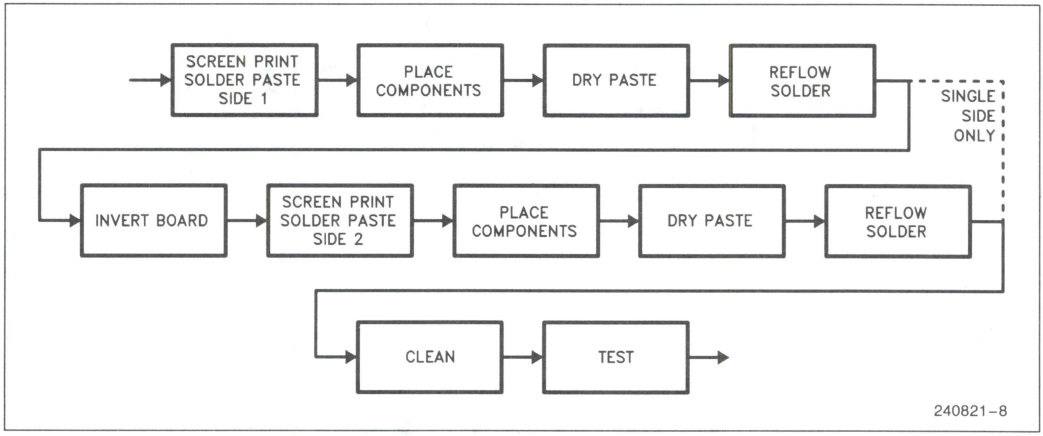


Figure 7-7. Typical Process Flow for Total Surface Mount (Type I SMT)

Type II assemblies go through the process sequence of Type I SMT followed by the sequence for Type III, as Figure 7-8 illustrates. In general practice only passive chip components are exposed to solder wave immersion.

There are three major process steps in the manufacturing of electronic assemblies: component mounting, soldering, and cleaning. For conventional as well as surface mount assemblies, the equipment required for each process step is shown in Figure 7-9. The equipment shown in "single box" in this figure is for conventional assemblies, and in "double box" for SMT. If Type III equipment is properly selected, it can be used for Type I and Type II SMT when the decision is made to move into those technologies.

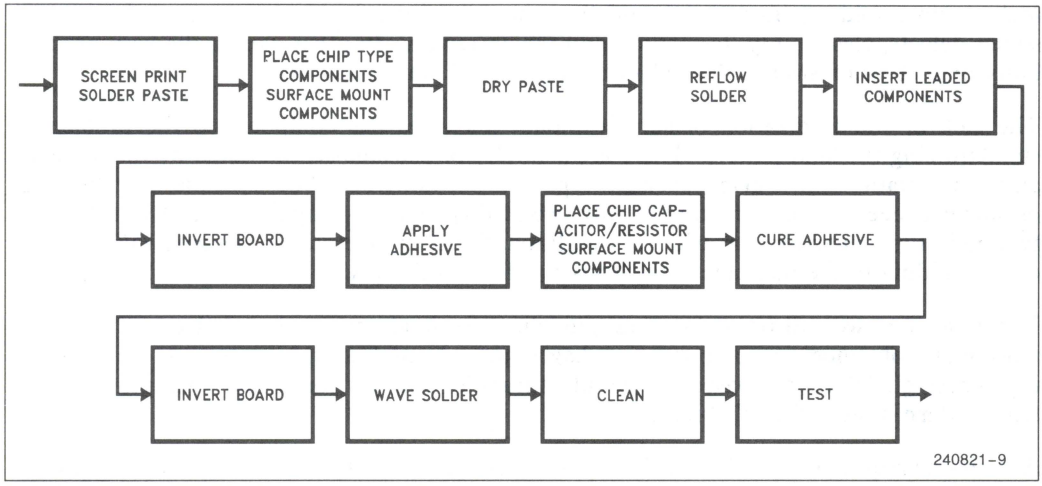


Figure 7-8. Typical Process Flow for Mixed Technology (Type II SMT)

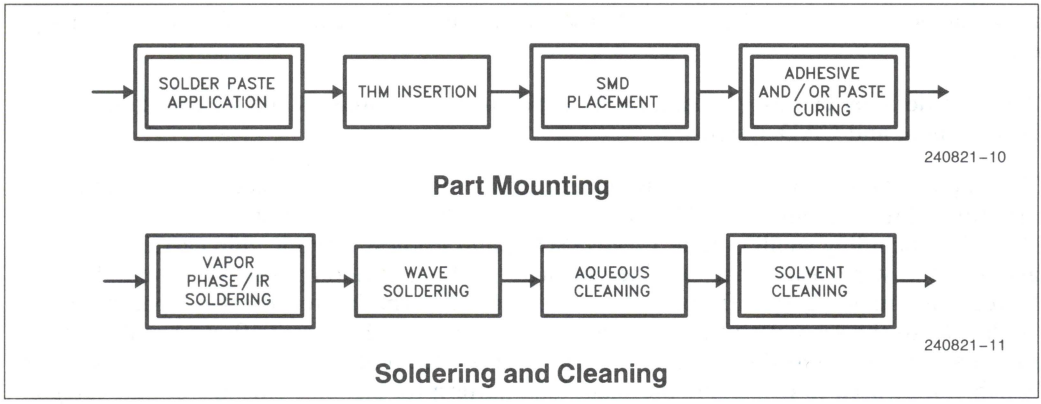


Figure 7-9. Major Equipment for Conventional (Single Box) and Surface Mount (Double Box) Assemblies (Type II SMT)

SMT manufacturing is modular in nature, and the full SMT capability can evolve in steps as needed. A line set up for Type II can be used for both Type I and Type III SMT.

SURFACE MOUNT DESIGN

Land Pattern Design

The surface mount land patterns, also called footprints or pads, define the sites where components are to be soldered to the PC board. The design of land patterns is very critical, because it determines solder joint strength and thus the reliability of solder joints, and also impacts solder defects, cleanability, testability, and repair/rework. In other words, the very producibility or success of SMT is dependent upon the land pattern design.

The lack of standardization of surface mount packages has compounded the problem of standardizing the land pattern. There are a variety of package types offered by the industry, and the variations in a given package type can be numerous. For example, for the small outline package (SOP), there are not only two lead types (gull-wing and J-lead), but there are two body types (narrow and wide). In addition, the tolerance on components varies significantly, adding to the manufacturing problems for SMC users.

In this section, we will present general guidelines for land pattern design that accommodate reasonable tolerances in component packages, process, and equipment used in manufacturing. These guidelines are based on manufacturability and environmental testing of different land pattern designs for reliability.

A desirable requirement is that the land pattern design be transparent to the soldering process used in manufacturing. This reduces the number of pad sizes in the computer-aided design (CAD) library—some CAD systems limit the total number of different pad sizes, but this may change with newer releases of CAD software—and is less confusing for the CAD designer.

Also, the designer can use the land pattern document to establish standard configurations for both manual and CAD systems.

To simplify the land pattern design guidelines, we have divided surface mount components into three different categories: (1) passive components; (2) J-lead plastic leaded chip carriers (PLCCs), including small outline J-leads (SOJs) and leadless ceramic chip carriers (LCCCs); and (3) gull-wing lead small outline packages (SOPs), including surface mount R-packs. Instead of providing specific pad sizes, the general formulas for the land pattern design applicable to the second and third categories are shown in Figures 7-10, 7-11 and 7-12. The formulas were developed based on reliability and producibility data. Each has a constant, K, which can be used to determine the exact land pattern for any size package in that category. References 2, 3, and 4 provide the details on land pattern design. Footprint areas for 80, 100 and 208 lead SQFP packages have been shown in Figure 7-13.

Table 7-1. Typical Board Footprint Area for PLCC

	Lead Count	A (Width) (Inch)	B (Length) (Inch)
Square	20	0.420	0.420
	28	0.520	0.520
	44	0.720	0.720
	52	0.820	0.820
	68	1.020	1.020
	84	1.220	1.220
Rectangular	28	0.420	0.620
	32	0.520	0.620

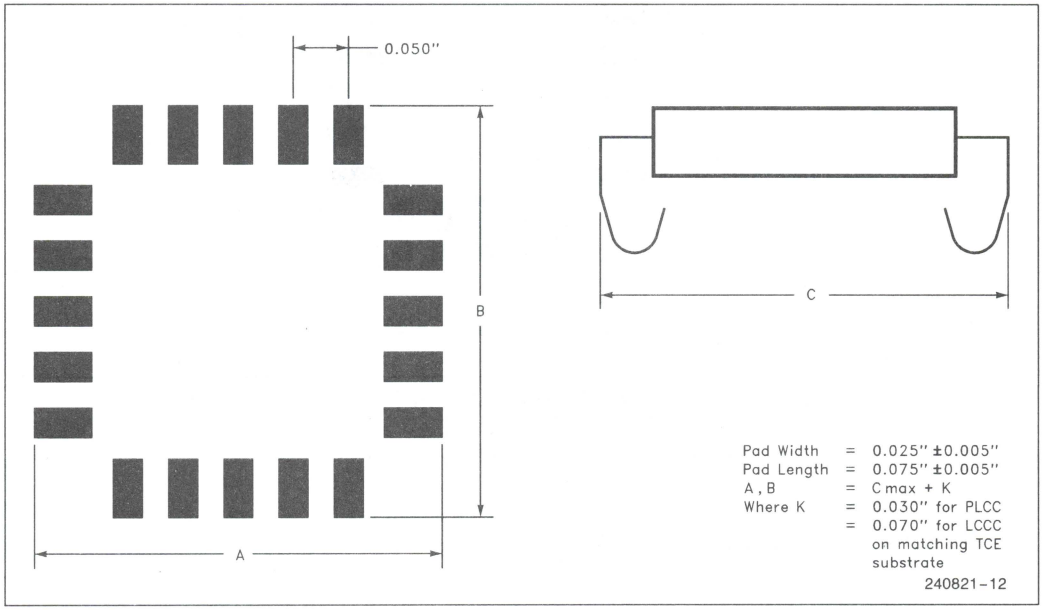


Figure 7-10. Typical PLCC, LCCC Footprint for Board Layout, Square and Rectangular Package

Table 7-2. Typical Board Footprint Area for PQFP

Lead Count	A (Width) (Inch)	B (Length) (Inch)
84	0.810	0.810
100	0.910	0.910
132	1.110	1.110
164	1.310	1.310
196	1.510	1.510

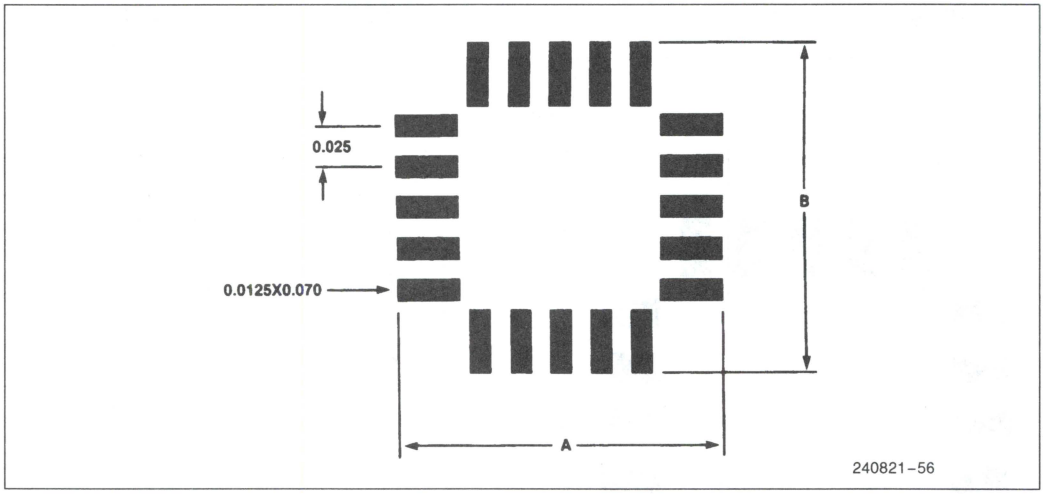


Figure 7-11. Typical PQFP Footprint for Board Layout

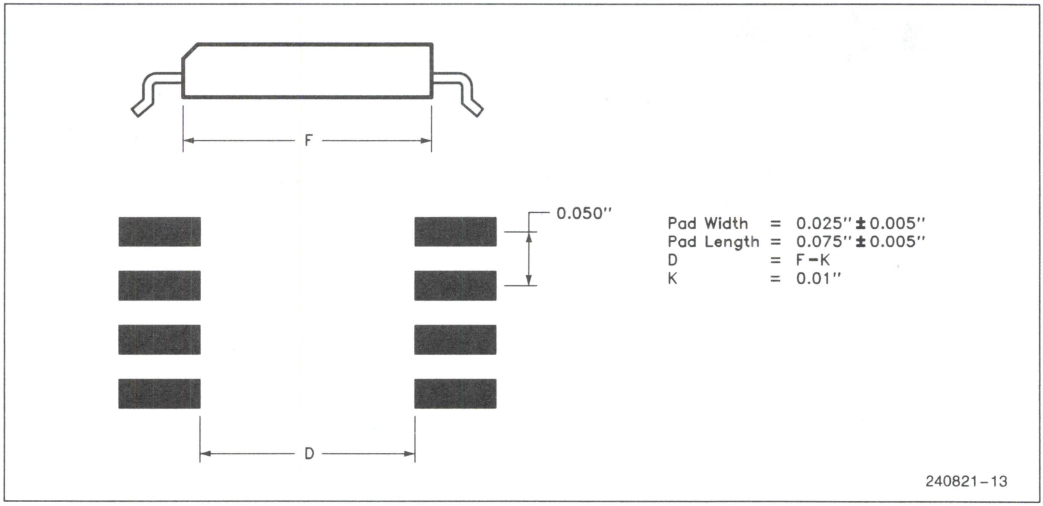


Figure 7-12. Formulas for R-Packs and SOIC Land Pattern Design

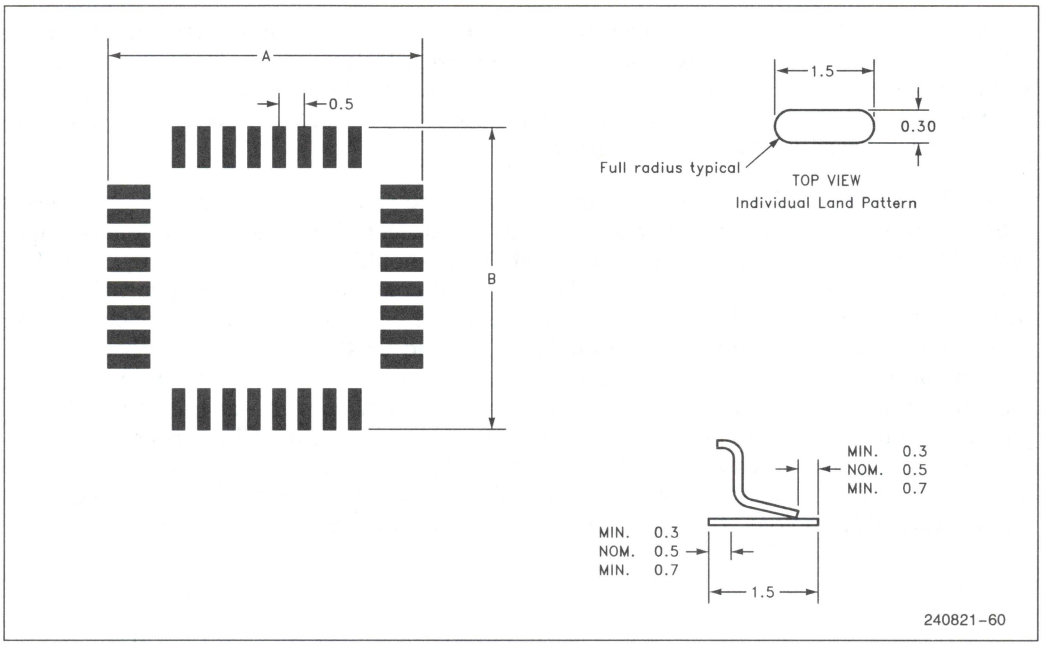


Figure 7-13. Typical SQFP Footprint for Board Layout

Table 7-3. Typical Board Footprint Area for SQFP

Lead Count	A (Width) (mm)		B (Length) (mm)	
	min	max	min	max
80 Lead SQFP	14.80	15.00	14.80	15.00
100 Lead SQFP	16.80	17.00	16.80	17.00
208 Lead SQFP	30.80	31.00	30.80	31.00

Design for Manufacturability

Design for manufacturability is gaining more recognition as it becomes clear that cost reduction of printed wiring assemblies cannot be controlled by manufacturing engineers alone. Design for manufacturability—which includes considerations of land pattern, placement, soldering, cleaning, repair, and test—is essentially a yield issue. Thus, companies planning surface mount products face a serious challenge in creating manufacturable designs, generally working by trial and error and at a considerable expense. Achieving decent yield can be a source of constant irritation and often total frustration.

Of all the issues in design for manufacturability, land pattern design and interpackage spacing are most important. Interpackage spacing controls cost-effectiveness of placement, soldering, testing, inspection, and repair. A minimum interpackage spacing is required to satisfy all these manufacturing requirements, and the more spacing provided, the better. The following guidelines meet manufacturability requirements.

Figure 7-14 shows the interpackage spacing between the pads (not component body or lead) of SMCs, as well as the spacing between the pads of adjacent SMCs and conventional components. The spacing from pad to pad of adjacent SMCs should be a minimum of 0.050 in. For PLCCs, this means 0.075 in. between leads of adjacent components. For components such as SOJs and passives, where leads or terminations are on only two sides of the packages, the interpackage spacing should be 0.050 in. for SOJs, and 0.040 in. for passives between the adjacent sides without leads or terminations. The spacing between the pads of conventional and surface mount components should be 0.060 in. to allow enough—at least a 0.100-in.—gap for auto-insertion equipment used for conventional components. Clear spaces of at least 0.050 in. should be allowed around all edges of the PC boards if the boards are tested off the connector, or of 0.100 in. if vacuum seal is used for testing, such as bed-of-nails. With current manufacturing technology, these specified requirements are absolute minimum.

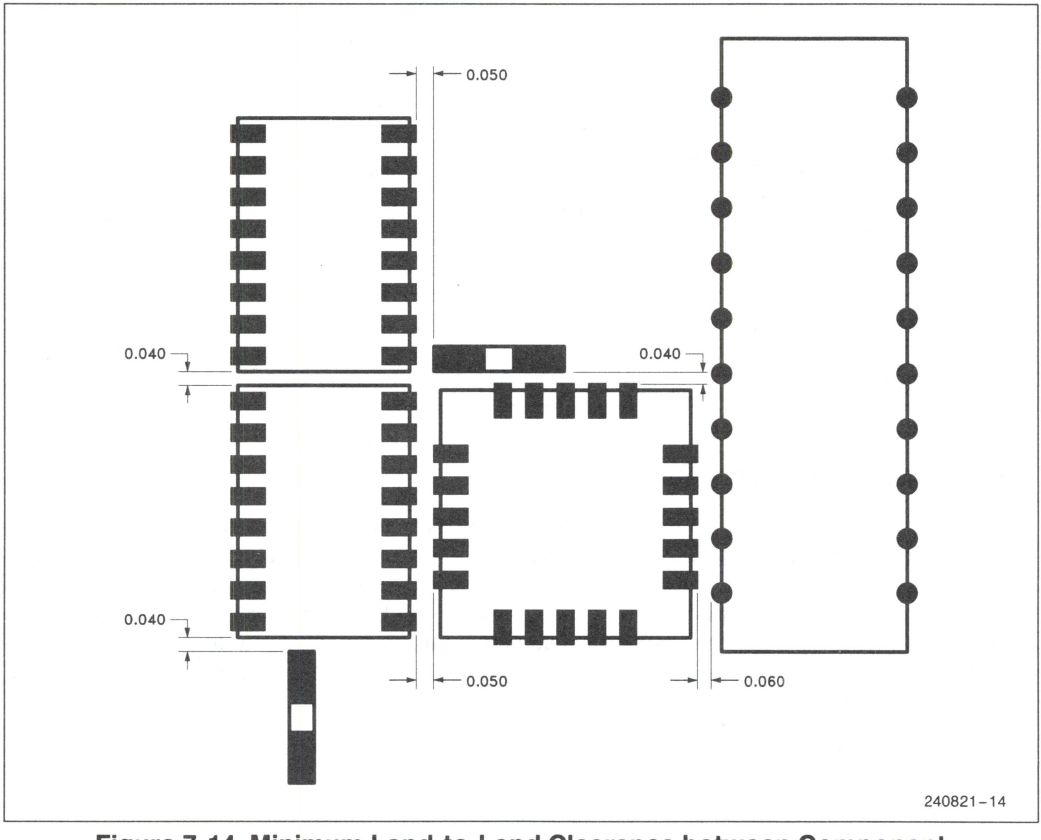


Figure 7-14. Minimum Land-to-Land Clearance between Component (Surface Mount and DIP) Lands

The interpackage spacing guideline just discussed may cause problems in some cases if the repair tool used in manufacturing does not use a vacuum tip for component removal and replacement during repair/rework. This problem may disappear when repair/rework with vacuum pick-up (removal and replacement) capability becomes available for both passive and active components. Currently, most of the available repair/rework tools are intended only for active devices.

Another manufacturing consideration is the alignment of components on the PC board. Similar types of components should be aligned in the same orientation for ease of component placement, inspection, and soldering.

Via holes are used to connect SMC lands to conductor layers. They may also be used as test targets for bed-of-nails probes and/or rework ports. Via holes may be covered with solder mask material if they are not required for node testing or rework. Such vias are called tented vias.

Via holes may be placed under surface mount components. However, in Type II and Type III SMT (mix-and-match surface mount), via holes under SMCs should be minimized or tented with solder mask to prevent trapping of flux under the packages during wave soldering. For effective cleaning, via holes should only be located beneath SMCs in Type I SMT assemblies (full surface mount) that will not be wave soldered.

Via holes within reflow-soldered pads should be avoided because solder can flow inside these vias during reflow soldering, causing insufficient solder fillets. Designing wide traces connected to solder pads produces the same effect as flush vias on solder pads—insufficient solder fillets.

Design for Testability

In SMT boards, designing for testability requires that test nodes be accessible to automated test equipment (ATE). This requirement naturally has an impact on board real estate. In addition, it impacts cost, which is dependent upon defects. A lower number of test nodes can be tolerated when defect rates are low, but higher defect occurrence demands adequate diagnostic capability by allowing ATE access to all test nodes.

Most companies use bed-of-nails in-circuit testing for conventional assemblies. Use of SMCs does not impact testability if the rule for testability of assemblies is strictly observed. This rule requires that (1) 0.050-in. and 0.100-in. test probes are used, (2) solder joints are not probed, and (3) through-hole vias or test pads are used to allow electrical access to each test node during in-circuit testing. If possible, this electrical access should be provided both at top and bottom, and bottom access is necessary. The main drawback of providing all the required test pads is that the real estate savings offered by SMT are somewhat compromised. To retain these savings requires development of some form of self-test or reliance upon functional tests only. However, self-test requires considerable development effort and implementation time, and functional tests lack the diagnostic capability of in-circuit tests.

Designing for manufacturability, test, and repair are very important for yield improvement and thus cost reduction. Design for manufacturability and test essentially impacts SMT real estate savings. If processes are brought under control, the need for repair and test will become

less of an issue, but until then, some real estate benefits provided by SMT and easily producible surface mount boards will be sacrificed. The following sections address process issues in the manufacturing of surface mount assemblies that play a critical role even when boards are designed for manufacturability.

SUBSTRATE PREPARATION: ADHESIVE, SOLDER PASTE APPLICATION

Solder Application, Paste, and Preform

Solder paste plays an important part in reflow soldering (Type I and Type II SMT). The paste acts as an adhesive before reflow and even may help align skewed parts during soldering. It contains flux, solvent, suspending agent, and solder of the desired composition. Characteristics such as viscosity, dispensing, screening, flux activity, flow, ease of cleaning, and spread are key considerations in selecting a particular paste. Susceptibility of the paste to solder ball formation and wetting characteristics are also important selection criteria.

Solder paste is applied on the solder pads before component placement by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh, and stencils are etched stainless steel or brass sheets. Stencils are preferred for high-volume product runs, because they are more durable than screens, are easier to align, and can apply a thicker layer of solder paste. Because they are more expensive than screens, they may not be suitable for small production runs.

The types of paste available fall under three main categories: rosin (most often used in RMA, rosin mildly activated) solvent soluble, organic acid (OA) water-soluble, and no-clean. Each of these has advantages and disadvantages as listed in the Table 7-4, and choosing one over the others greatly depends on the application and the product type.

Table 7-4. Comparison of Solder Paste Types

Type	Advantages	Disadvantages
Rosin	— Stable Chemistry — Good properties	—Needs CFC solvent or saponification for cleaning
Water Soluble	— Cleaned using pure water — Very good cleanability — Other properties good when used within shelf life	— New products with evolving chemistries — Humidity sensitive, seen as: Short shelf and working life, solder ball tendency, and finally, deactivated flux
No-Clean	— No cleaning process, equipment, — or chemicals — Eliminates any effluent issues	— Lower activity — More difficult to control process — May leave some visible residue behind

SURFACE MOUNT COMPONENTS AND THEIR PLACEMENT

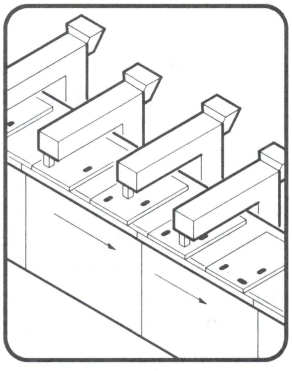
Component Packaging

All active components are not currently available in surface mount, which will keep us in mix-and-match format for some time to come. However, the situation is changing very rapidly.

Intel active components are available in tubes or trays, as well as tape and reel. The EIA specification RS-481A has standardized 7-in. reels for passive components and 13-in. reels for active components.

Component Placement

Requirements for accuracy make it almost mandatory to use auto-placement machines for placing surface mount components on the PC board. Selection of the appropriate auto-placement machine is dictated by the type of parts to be placed and their volume. As shown in Figure 7-15, there are basically four types of auto-placement machines available on the market today: (1) in-line, (2) simultaneous, (3) sequential, and (4) sequential/simultaneous placement equipment.



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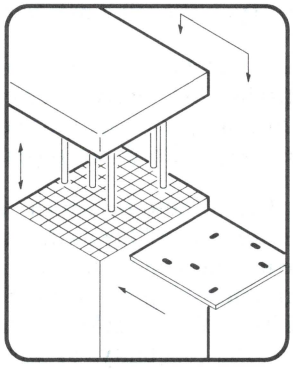
- Moving board/fixed head
- Each head places one component
- 1.8 to 4.5 seconds/board

a. In-Line Placement Equipment



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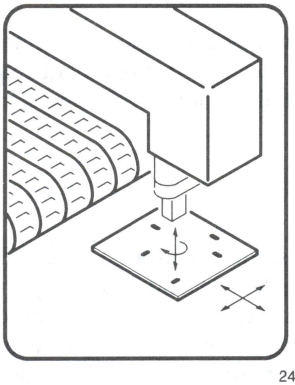
- Fixed table/head
- All components placed simultaneously
- Seven to 10 seconds/board

b. Simultaneous Placement Equipment



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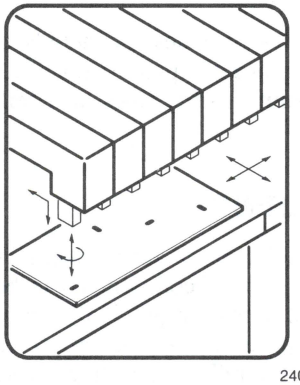
- X-Y movement of table/head
- Components placed in succession individually
- 0.3 to 1.8 seconds/component

c. Sequential Placement Equipment



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- X-Y table/fixed head
- Sequential/simultaneous firing of heads
- 0.2 seconds/component

d. Sequential/Simultaneous Placement Equipment

Figure 7-15. Four Major Categories of Placement Equipment

Shown in Figure 7-15, in-line placement equipment employs a series of fixed-position placement stations. Each station places its respective component as the PC board moves down the line. Cycle times vary from 1.8 to 4.5 seconds per board.

Illustrated in Figure 7-15, simultaneous placement equipment places an entire array of components onto the PC board at the same time. Typical cycle times vary from seven to 10 seconds per board.

Sequential placement equipment, shown in Figure 7-15, typically utilizes a software-controlled X-Y moving table system. Components are individually placed on the PC board in succession. Typical cycle times vary from 0.3 to 1.8 seconds per component.

Sequential/simultaneous placement equipment, illustrated in Figure 7-15, features a software-controlled X-Y moving table system. Components are individually placed on the PC board from multiple heads in succession. Simultaneous firing of heads is possible. Typical cycle times vary, with an average of 0.2 seconds per component.

Many models of auto-placement equipment are available in each of the four categories. Selection criteria should consider such issues as what kind of parts are to be handled; whether they come in tube, trays, or tape and reel; and whether the machine can accommodate future changes in other shipping media. Selection and evaluation of tapes from various vendors for compatibility with the selected machine is very important. Off-line programming, teach mode, and edit capability, as well as ECAD/CAM compatibility may be very desirable, especially if a company has already developed an ECAD/CAM database. Special features such as vision capability, adhesive application, component testing, board handling, and capability for further expansion may be of interest for many applications. Vision capability is especially helpful in accurate placement of fine-pitch packages. Reliability, accuracy of placement, and easy maintenance are important to all users.

Reference 4 provides the details on selection criteria for pick-and-place equipment. Since pick-and-place equipment constitutes the major portion of the capital investment required for SMT manufacturing lines, a detailed evaluation is essential before purchasing a particular machine.

SOLDERING

Like the selection of auto-placement machines, the type of soldering process required depends upon the type of components to be soldered and whether leaded and leadless parts will be combined. For example, if all components are surface mount types, the reflow method (vapor phase or infrared) may be desirable. However, for a combination of leaded and surface mount components, reflow soldering for surface mount components followed by wave soldering for through-hole mount components is optimum. No process is best for all soldering tasks. For example, in infrared reflow, both the heating and cooling rates of assemblies can be controlled more precisely than in vapor phase. This has a direct impact on solder defects, as discussed later.

Vapor Phase Soldering

Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid. The latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid. Thus, unlike wave, infrared, and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the PC board. It heats independent of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. The process is also suitable for soldering odd-shaped parts, flexible circuits, and pins and connectors, as well as for reflow of tin-lead electroplate and surface mount packages. However, all these features make vapor phase soldering an easily automated process. It does not require the fluxing, preheating, and soldering adjustments so critical in other processes. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, leads on packages heat up faster than the component body or solder pads. With leaded components, this can lead to the wicking of solder paste up the lead, causing open solder joints. Vapor phase soldering also has other process-related problems, such as solder balls, part movement, and damage to temperature-sensitive parts. Maximum temperature ramps rate can be controlled through the use of a preheat zone. For moisture sensitive PSMC a maximum allowable ramp rate has been recommended—see Table 9-1.

Both in-line and batch-type systems are available. The in-line system is suitable for mass production. For low-volume production or for research and development, a batch process is generally used. A schematic of a batch-type process is shown in Figure 7-16, and an in-line process in Figure 7-17. For both processes, the major disadvantages are price of the liquid, vapor loss, and parts movement (which can be advantageous for part alignment). The batch process minimizes vapor loss by using a less expensive secondary fluid as a blanket over the primary fluid. Alternative materials to CFC's containing secondary fluids have recently become available on the market. The cooling coils shown in Figure 7-17 are also intended to minimize vapor loss.

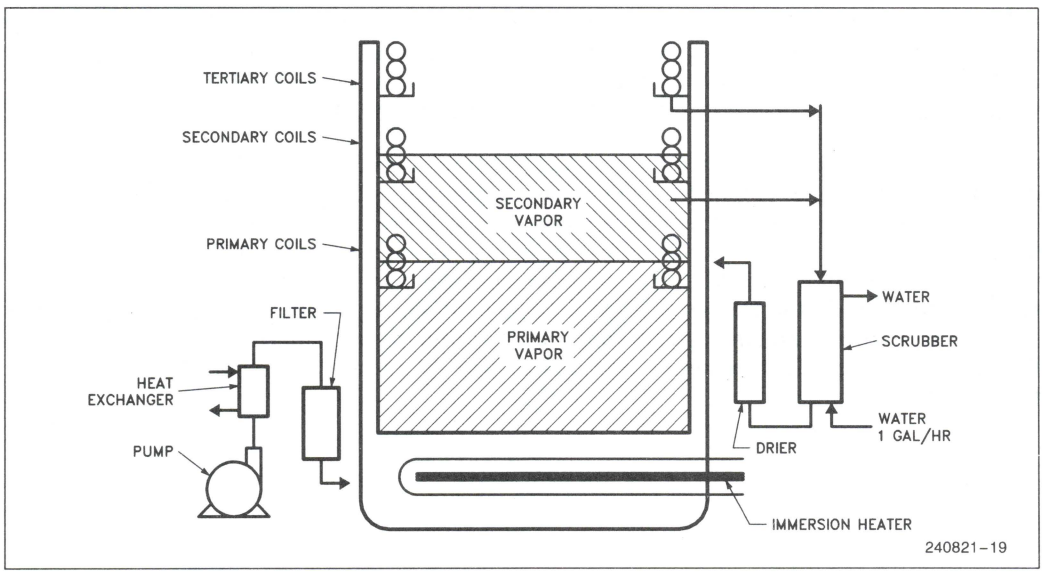

Figure 7-16. Schematic—Batch-Type Vapor Phase Soldering System for SMT

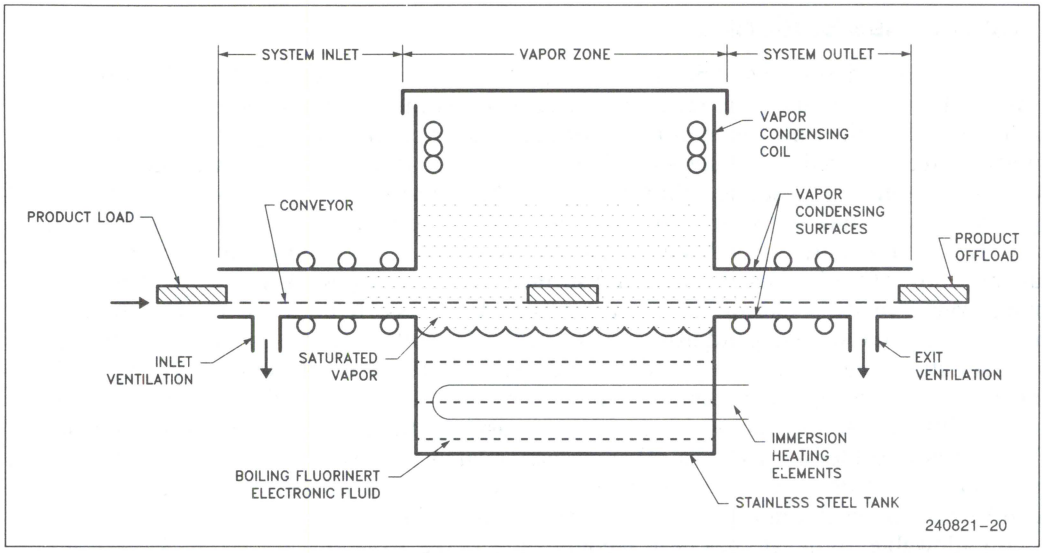

Figure 7-17. Schematic—In-Line Vapor Phase Soldering System for SMT

Infrared Reflow Soldering

In infrared (IR) reflow soldering, radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow processes: focused (radiant) and non-focused (convective). The latter is proving to be more desirable for SMT. Focused IR radiates heat directly on the parts and may heat assemblies unevenly. The heat input on the part may also be color-dependent. In non-focused or diffused IR, the heating medium can be air, an inert gas, or simply convection energy. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. The gradual heating of boards is accomplished by various top and bottom heating panels, as shown in Figure 7-21. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled. The solder paste used for vapor phase may not necessarily be suitable for the IR process.

The IR reflow process is generally considered more suitable for SMT packages. There is concern that packages supplied by some companies may not be compatible with certain IR ovens. The advantage of IR over vapor phase is that, if properly designed, it can be used for baking adhesive and paste, and for reflow soldering. Another key advantage of IR over vapor phase is the operating cost. Also, the incidence of solder joint openings due to lead coplanarity is less frequent in the IR process than in vapor phase (see References 4 and 5). As in the case of VPS a maximum temperature ramp rate has been recommended for moisture sensitive PSMC—see Table 9-1. Because of these reasons, the IR process is becoming very popular in the United States.

Hot Bar Reflow Soldering

The ability to place and reflow high lead count, ultra fine pitch components challenges traditional stencil, place and reflow (SPR) processes such as infrared and vapor phase reflow soldering at or below 0.4mm lead pitch. This is due to the solder paste flow characteristics through very small stencil apertures and mechanical alignment difficulties with stencil to substrate. Pulsed resistance thermode attachment or "hot bar" reflow is an outer lead bonding technique currently being developed for component lead pitches down to 0. 2mm.

Current component input into the placement system can be accomplished through many different format types; molded carrier ring, singluated slide carriers, or matrix trays. Liquid flux is applied to each side of the component on a thin film of flux for better heat transfer and oxidation prevention. Each side is coated individually to prevent flux from adhering to the bottom side of the component. No-clean "low solids" fluxes that can withstand the higher temperature of the thermodes (approx. 300C–350C) without carbonizing are recommended for this application. An advanced machine vision system is used to perform component lead inspection, board fiducial location and calculate placement location. After component placement, the hot bar blades are brought down to "gang bond" all the leads simultaneously. The blades physically contact the top of the component leads, holding them in place during reflow and cool down. The configuration is shown in Figure 7-19. This hold down process results in fewer problems due to coplanarity. Heat is conducted through the leads and into the solder deposit to form solder fillets. The blades are then allowed to cool to let the solder re-solidity before lifting. Computer control manages the temperature and force profiles for each component type. Different thermal masses make this essential. A sample profile is shown in Figure 7-20.

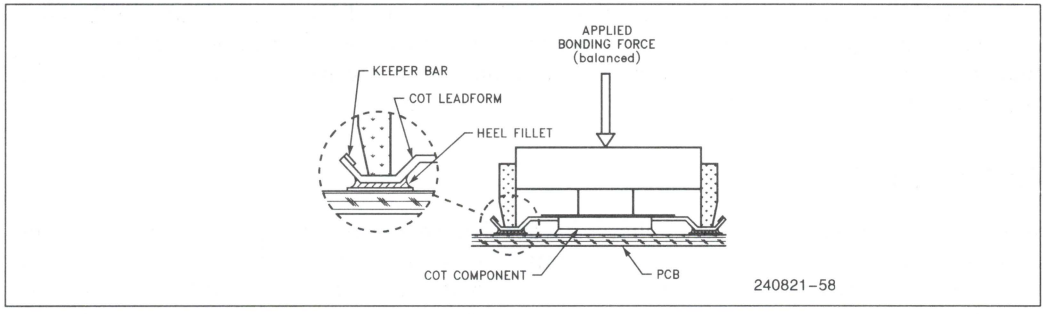

Figure 7-19. Hot bar soldering setup. Leads are held down on the lands during the reflow/cool cycle

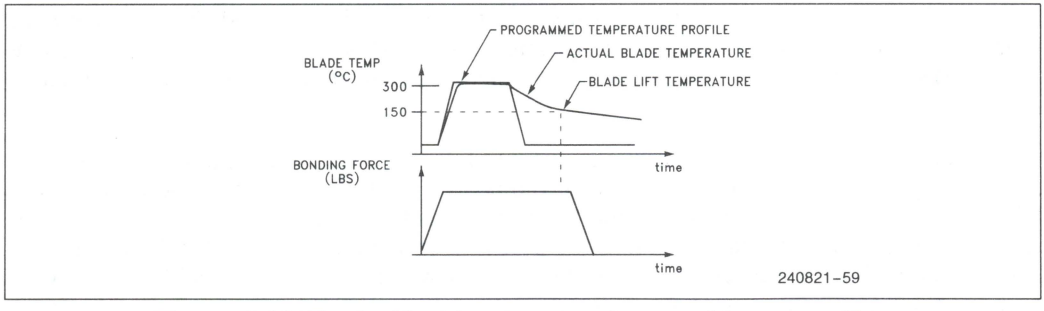

Figure 7-20. Typical hot bar temperature and force profiles

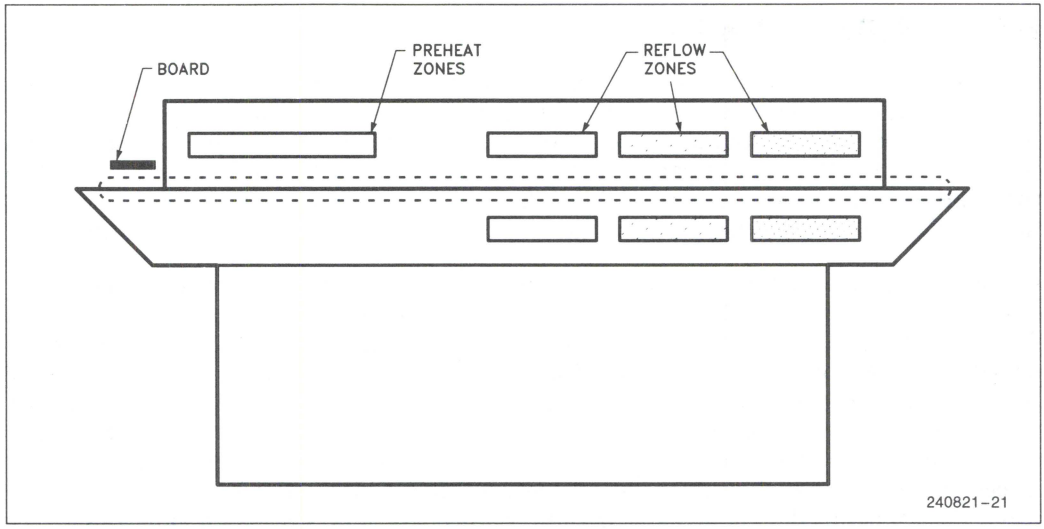

Figure 7-21. Schematic—In-Line Infrared (IR) Soldering System for SMT

Laser Reflow Soldering

Laser soldering is a relative newcomer to soldering technology. It complements other soldering processes rather than replacing them, and like vapor phase and IR soldering, lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, or IR soldering. Heat-sensitive components that might be damaged by vapor phase or IR can be soldered easily by laser since only the leads are heated to reflow temperature. In laser soldering, the process problems involve potential damage to adjacent components if laser beam width is not properly adjusted.

CLEANING

In general, cleaning of SMT assemblies is harder than that of conventional assemblies because of smaller gaps between surface mount components and the PWB surface. The smaller gap can entrap flux, which can potentially cause reliability problems if the PWB is not properly cleaned. Thus, the cleaning process depends upon the spacing between component leads, spacing between component and substrate, the source of flux residue, type of flux, and the soldering process. Most companies use synthetic or rosin-based fluxes generally known as rosin activated (RA), rosin mildly activated (RMA), synthetic activated (SA), or synthetic mildly activated (SMA). Stabilized halogenated hydrocarbon/alcohol azeotropes, such as freon TMS, or saponfier are the preferred solvents for removal of synthetic and rosin-based flux residues.

Some companies successfully use organic acid (OA) flux for wave soldering of passive surface mount components glued to the bottom of the board (see Reference 6). Residues from OA fluxes are generally removed with water. Success of this technique is usually directly proportional to the amount of adhesive filling the potential entrapment area under the component and pressure of the water jets in the cleaner. Use of water-soluble fluxes will be increasing because they are environmentally more desirable. Also, due to recent efforts to reduce

chlorofluorocarbons (CFCs) to prevent ozone layer depletion, water-soluble fluxes and solvents with no CFCs are becoming mandatory. Environmental concern is also driving the usage of water-soluble solder paste, and no-clean solder paste.

One of the key issues in SMT has been to determine cleanliness of SMT assemblies, because the conventional Omega meter test used for DIP boards may not be adequate. For this reason, the industry is trying to standardize on surface insulation resistance (SIR) surface mount boards. The current industry standard for board cleanliness is 100-megohm SIR after cleaning, regardless of which flux or cleaning method is used.

REPAIR/REWORK

Repair/rework of SMT assemblies is easier than that of conventional components. Due to the absence of plated through-holes, these components are easier to remove, and the possibility of thermal damage is decreased. A number of tools are available for removing components, including hot-air devices for removing active surface mounted components. A key issue in using hot-air devices is preventing thermal damage to the component or adjacent components.

No matter which tool is used, all the controlling desoldering/soldering variables need to be addressed, including the number of times a component can be removed and replaced, desoldering temperature and time, and damage to PWAs. It is also very helpful to preheat the board assembly at 150°F–200°F for 15 to 20 minutes before rework to prevent thermal damage such as measling or white spots of the boards, and to avoid pressure on pads during the rework operation (see Reference 7). To prevent moisture induced damage, SMT components may require bake-out prior to removal from the board. The guidelines outlined in the Dessicant Pack Section should be followed.

TECHNICAL ISSUES IN FINE PITCH

The need for high lead-count packages in semiconductor technology has increased with the advent of application-specific integrated circuit (ASIC) devices and increased functionality of microprocessors. As the package lead count increases, devices will get larger and larger. To ensure that the area occupied by packages remains within limits of manufacturing equipment, lead pitches have been reduced. This—coupled with the drive toward higher functional density at the board level for enhanced performance and miniaturization—has fostered the introduction of many devices, such as Intel486™ SX microprocessor, in fine-pitch surface mount packages.

A fine-pitch package can be broadly defined as any package with a lead pitch finer than the 50-mil lead pitch of standard surface mount packages as PLCCs and SOPs. Most common lead pitches are 25 mils, but lower pitch devices are also becoming available in pitches of 0.5mm and some QFP's are now available in 0.4mm pitch.

There are two different versions of fine-pitch packages: those with corner bumpers and those without. Versions without bumpers are called quad flatpacks (QFPs); those with bumpers are referred to as plastic quad flatpacks (PQFPs). The QFP types have a very low stand-off height, making it very difficult to clean assemblies containing these packages.

The assembly process most dramatically affected by the fine-pitch package is component placement. Placement of any surface mount package with 25 mils or less of lead pitch must be made with the assistance of a vision system for accurate alignment.

Placement vision systems typically consist of two cameras. The top camera system scans the surface of the board and locates three fiducial targets that are designed into the artwork of the board. The placement system then offsets the coordinates in the computer for any variation in true board location. The bottom camera system, located under the placement head, views the component leads. Since the leads of fine-pitch components are too fragile to support mechanical centering of the device, the vision system automatically offsets for variations in the X, Y, and theta dimensions. This system also inspects for lead integrity problems, such as bent or missing leads.

The manufacturing issues for assembling fine-pitch components on PC boards also include (1) printing various amounts of solder paste on the 25-mil and 50-mil lands, (2) soldering and inspecting the fine-pitch leads and solder joints, (3) reworking defective devices, (4) cleaning adequately under and around package leads, (5) baking of the packages to remove moisture, and (6) handling of the packages without damaging fragile leads. These challenges are by no means insurmountable, but require investment in capital and engineering resources.

CONCLUSION

The major technical considerations for implementing SMT include surface mount land pattern design, design for manufacturability, components and their placement, adhesive-application wave soldering, reflow soldering, cleaning, and repair/rework. These considerations must be taken into account and thoroughly understood before converting to SMT. Surface mount technology is revolutionary, and for most companies, requires a complete rethinking of design and manufacturing processes, including the software and tool methodologies used to support them. SMT is not a technology of tomorrow, but a technology of today. Intel has made the investment in SMT for component, board, and system products to keep customers on the leading edge.

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6. R. Aspandiar, A. Piyarali, R. Prasad: "Is OA OK?" *Circuits Manufacturing,* April 1986, pp. 29-36.
7. R. Prasad: "Contributing Factors for Thermal Damage in PWB Assemblies During Hand Soldering," *IPC Technical Review,* January 1982, pp. 11-12.

REVISION SUMMARY

The main differences between 240821-004 revision and the -003 version are the following:

- Added SQFP Land Pattern

Moisture Sensitivity/ Desiccant Packing/Handling of PSMCs

8

CHAPTER 8
MOISTURE SENSITIVITY/DESICCANT PACKING/HANDLING OF PSMCs

INTRODUCTION

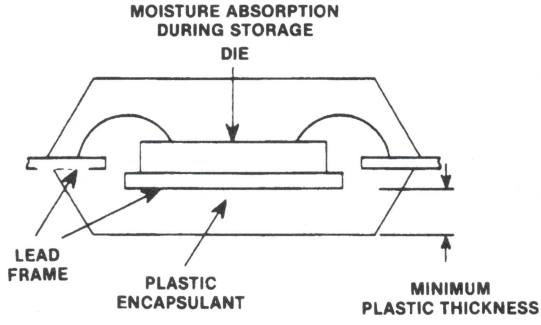
This chapter of the Packaging Handbook examines surface mount assembly processes and establishes a standard preconditioning flow which encompasses moisture absorption, thermal stress and chemical environments typical in the variety of surface mount assembly methods currently in use. Moisture absorption/desorption characteristics are reported and cracking danger levels are assigned to products identified as moisture sensitive by Intel. Baking to reduce package moisture level, and its potential effect on lead finish solderability is described. In addition, drying, shipping, and storage procedures are included for plastic surface mount component (PSMC) packages, which are susceptible to moisture related failure mechanisms in user's surface mount manufacturing processes.

MOISTURE SENSITIVITY OF PSMCs

There are a number of technical issues that need to be understood with regards to maintaining package integrity during board level assembly processing using Plastic Surface Mount Components (PSMC). Surface mount processing subjects the component body to high thermal exposure and chemicals from solder fluxes and cleaning fluids during users' board mount assembly. In through-hole technology the board assembly process uses wave soldering which primarily heats the component leads. The printed circuit board acts as a barrier protecting the DIP package body from solder heat and flux exposure. See Figure 8-2. In order to assure PSMC package integrity throughout the surface mount process, precautions must be taken by both supplier and user to minimize the effects of reflow solder stress on the component. Plastic molding compounds used for integrated circuit encapsulation are hydroscopic and absorb moisture to a level dependent on the storage environment. Stress results from thermal expansion mismatch between the plastic encapsulant and the metal lead frame. This can lead to loss of encapsulant adhesion to the die and the lead frame. Absorbed moisture can segregate at these separate interfaces, vaporize during rapid heating in the solder reflow process, generating pressure at various interfaces in the package, followed by swelling and finally cracking of the plastic, as illustrated in Figure 8-1. Cracks can propagate either through the body of the plastic or along the lead frame (delamination). Subsequent high temperature exposure and moisture in the package can induce the transport of ionic contaminants through these openings to the die surface increasing the potential for circuit failure due to corrosion.

It should be noted that the PSMC moisture sensitivity relates only to risk associated with direct exposure of components to reflow solder process stresses. No loss of package integrity is expected for socketed parts or for through-hole mounted components *not subjected to solder reflow environment.* If through-hole components are exposed to SMT processing they can exhibit the same moisture sensitivity as PSMCs. If through-hole devices are exposed to solder reflow processes such as VPS or IR, they should be baked dry first, using the same baking procedures described in this book for SMT packages. Current data indicates there is no negative long term effects on reliability of PSMCs when package integrity is maintained through surface mount processing.

The effect of moisture in PSMC packages and the critical moisture content which will result in package damage or failures is a complex function of several package design and material property variables. These include: silicon die size, encapsulant thickness, encapsulant yield strength, encapsulant adhesive strength and thermal expansion properties of materials used in the package. The PSMC moisture sensitive phenomenon has been identified as a contributor to delamination related package failure mechanisms including bond lifting, wire necking and bond cratering, as well as die surface thin film cracking, and other problems. Package cracking is commonly treated as the most visible and severe form of moisture sensitivity. If package cracking is evident, the other failure mechanisms may also be present to some degree. Intel has evaluated PSMC crack jeopardy for its current portfolio. Package moisture level has been measured as a function of temperature and relative humidity. Critical moisture level limits to avoid cracking have been determined and products susceptible to cracking have been identified. Intel implemented handling procedures to assure that these products are delivered to users so that packages will not crack during user solder reflow processing. The user must take responsibility during storage, board mount assembly and board rework to avoid package over exposure to moisture by following precautions recommended in the following pages. These steps are necessary to assure package integrity is maintained throughout the surface mount process.



MOISTURE SATURATES THE PACKAGE TO A LEVEL DETERMINED BY STORAGE RH, TEMPERATURE, TIME AND PLASTIC MOISTURE EQUILIBRIUM SOLUBILITY.

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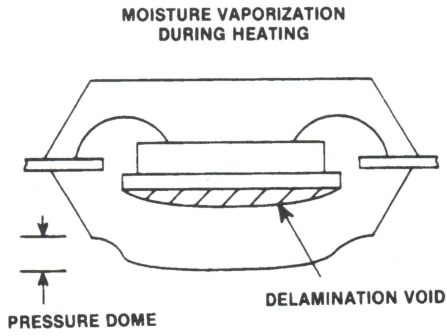
CRACK GENERATION DURING SOLDER



VAPOR PRESSURE AND PLASTIC EXPANSION COMBINE TO EXCEED ADHESIVE STRENGTH OF PLASTIC BOND TO LEAD FRAME DIE PAD. PLASTIC DELAMINATES FROM PAD AND VAPOR-FILLED VOID EXPANDS, CREATING A CHARACTERISTIC PRESSURE DOME ON THE PACKAGE SURFACE

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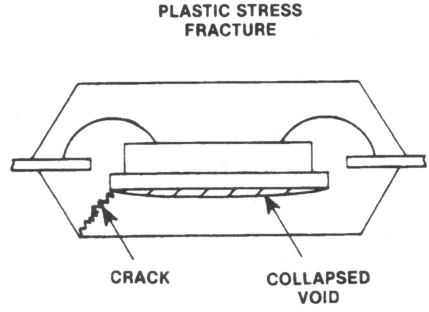

CRACK FORMS AND PRESSURE DOME COLLAPSES, EMANATING FROM BOUNDARY OF DELAMINATION AREA AT FRAME PAD EDGE. REMAINING VOID AREA ACTS TO CONCENTRATE STRESSES IN SUBSEQUENT TEMPERATURE CYCLING, LEADING TO FURTHER CRACK PROPAGATION.

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Figure 8-1. Package Crack Mechanism

8

Surface Mount Assembly Processes

Traditional insertion (through-hole) assembly technology involves relatively few process steps and minimizes the exposure of components to harsh processing environments. Modern surface mount assembly can be very complex, especially if mixed technologies (surface mount and insertion) are used on the same board. Furthermore, the components are fully immersed in the solder heating media (vapor phase or infrared reflow) in surface mount mass reflow processes whereas solder heat during solder dip (or wave solder) is applied only to leads of insertion mount packages. The circuit board shields the package body from the heat of the solder wave. Component exposure in both vapor phase and wave solder process environments is illustrated in Figure 8-2.

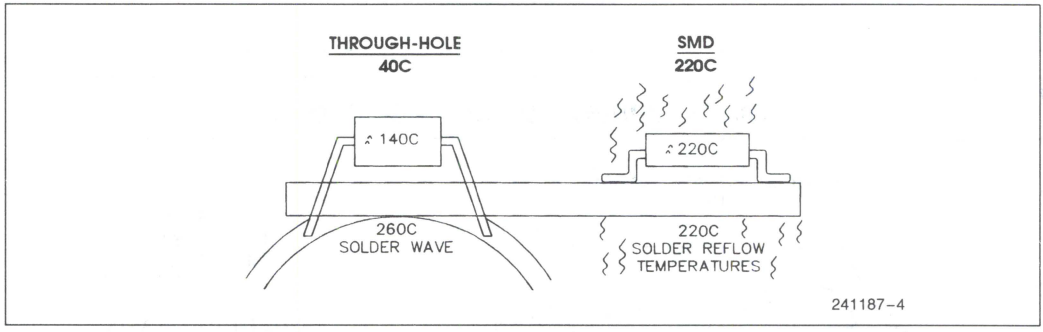


Figure 8-2. Component Exposure to Wave Solder and Vapor Phase Environments

Solder Reflow Processes; IR, VPS, and Hot Bar

Numerous solder processes are used in attaching components to boards. These range from manual soldering of individual leads with a soldering iron to high volume mass bonding techniques. The three most popular production methods are: vapor phase soldering (VPS), infrared reflow soldering (IR) and hot bar. *Vapor Phase* soldering uses the latent heat of condensation of a vapor to provide heat for soldering. This latent heat is transferred to the component as the vapor of the inert liquid condenses on the component. The VPS temperature reaches its maximum possible value at the fluid boiling point (215°C). The maximum heating rate of the component on the board occurs when it is initially immersed in the primary vapor, hence control of heating rate for any part is limited to preheating the part before immersion in the primary vapor zone. *IR solder reflow* processing uses radiant heating to provide heat for soldering. IR panels heat the board traveling on the conveyor from top and/or bottom. A gradual heating of the printed circuit board which is necessary to drive off the volatile constituents of the solder paste assures a controlled heating rate. After an appropriate preheat time, the board is raised to the reflow temperature for soldering and then carefully cooled down. *Hot Bar* (Thermode): This is a relatively new process that will handle smaller to midsize volumes of SMD's. The principle is simple in that the component's leads are held in direct contact to a heated clamp or holding device that presses the component into the solder paste and heats the leads to the reflow temperature. The advantage is that the plastic body does not experience the temperature extremes of a full reflow process. This is useful for very heat sensitive components or very small volume production that does not warrant the purchase of production machinery and moisture sensitive storage equipment. This equipment is useful in lab and prototype work. (See Chapter 9 Figure 9-2).

Thermal Shock on Components (Vapor Phase versus IR)

Rapid heating and cooling rates also cause thermal shock if there is insufficient time for the center and surface of components to reach the same temperature. Surface temperature, being higher than the internal body temperatures during heating, results in a temperature differential which generates thermo-mechanical stress. The degree of thermal shock on components is usually higher in VPS than in IR. The IR soldering profile is usually designed to heat the components at a rate of 2°C–6°C per second. Only a limited control can be exerted on the heating rate of components and boards in VPS. The maximum heating rate during VPS is typically much higher (up to 25°C/second). Such high rates of temperature increase can damage PSMCs simply because of the differences in thermal coefficient of expansion (TCE) mismatch between materials. This problem is exacerbated when components have been allowed to become moisture saturated.

NOTE:
No component body should ever be exposed directly to the wave solder during the wave solder operation.

Intel has determined guidelines for mass reflow soldering and post solder reflow component rework which (see Chapter 9 Figure 9-2) if followed will minimize thermal shock to packages and meet users' solder reflow requirements.

Solder Fluxes

Flux used in solder paste or in board pre-tinning processes is a major source of ionic contamination which can corrode IC chip metallization if transported to the chip surface. Those fluxes containing hydrochloric acid or other halogen compounds should be avoided. (Intel's processes are completely halide free.) Special cleaning methods to assure complete removal of all flux residues should be implemented where use of these materials is selected or required. Highly active fluxes such as organic acid (OA) types should be avoided. RMA or lower activity fluxes should be used whenever possible.

Because of the drive to eliminate CFC containing materials in solder flux removal, alternative cleaning methods have been under development. Terpene based materials have not shown to cause any long term effects with PSMC components. A relatively recent development is the no-clean or low clean fluxes. These require virtually no cleaning other than a water rinse of the board following SMT reflow. Another method of fluxing with inert gases is being introduced and could hold promise in the future for many companies.

ULTRASONIC CLEANING OF I.C. COMPONENTS

Various equipment companies are promoting the use of ultrasonic cleaning equipment to remove flux and other residues from the finished boards. Intel has found no evidence that would link the use of Ultrasonic cleaning to any type of immediate or latent failures in molded plastic components. Therefore, there seems to be no reason to discourage the use of ultrasonic cleaning on plastic components when cleaned in a standard procedure as listed in Table 8-1.

However, with Ceramic or Hermetic packages (that have an internal cavity), older, higher power ultrasonic equipment has shown some damage to the internal bond wires and solder joints when exposed to long cleaning times. Most of these problems have been overcome with the use of the newer lower power equipment. Each component's user must evaluate their application in light of the criteria in Table 8-1 to determine any reliability jeopardy to the boards.

Ultrasonic cleaning is not approved for devices that are still being studied. These are: Cerdip packages with very long wire lengths and PGAs. Information on these packages will be made available when the studies are complete.

Table 8-1. Ultrasonic Cleaning

Power of Ultrasonic Cleaner	< 30 Watts per Liter
Ultrasonic Range	39 KHz to 66 KHz
Cleaning Time	3 Minutes per Cycle for 5 Cycles Not to Exceed a Total of 15 Minutes

Solderability

Intel currently supplies PSMCs with copper lead frames and solder plated (tin/lead) finished leads. A potential for lead finish solderability degradation can occur due to formation of Cu_6Sn_5 intermetallic which does not dissipate during the solder reflow cycle. In order to meet users' solderability requirements the formation of intermetallics must be minimized. Intel has performed evaluations to determine solderability degradation of PSMC after burn-in and baking, which is necessary to drive out package moisture prior to sealing sensitive products in moisture barrier bags (MBBs). *Based on the solderability work done at Intel it is recommended that PSMC product be baked at high temperature (125°C) no more than 24 hours by the user.* Intel monitors outgoing solderability to assure that product meets user's solderability requirements.

Conclusion

Component susceptibility to moisture damage can manifest itself in many ways. Some of these can be package cracking, bond lifts, die surface thin film cracking, bond cratering or severe delamination. Package cracking is one of the most severe forms of moisture sensitivity. Package cracking has been correlated to be a function of die and package geometry and is aggravated by moisture absorption in the plastic encapsulant. Moisture damage to crack susceptible components can be minimized through users processes if absorbed moisture is kept below critical levels and surface mount process thermal limits are observed. Maximum temperature profiles are recommended for these solder processes to minimize crack jeopardy due to thermal stresses. Moisture absorption and desorption characteristics of these sensitive packages have been characterized and moisture exposures sufficient to induce moisture damage have been determined. **Intel bakes PSMC packages dry and seals them in bags with desiccant before shipping*.** Recommended shelf life, storage conditions, redrying and handling procedures are described on the bag and in this Packaging Handbook. The user must limit exposure of moisture sensitive components to environmental moisture during SMT assembly and rework processing in order to keep absorbed moisture below recommended limits and assure package integrity is maintained throughout the assembly process.

*32-lead and 40-lead TSOP packages are not shipped in bake and bag.

GUIDELINES FOR HANDLING UNITS IN DESICCANT PACK

Intel will ship moisture sensitive plastic surface mount components (PSMCs) in a dry state inside moisture barrier bags (MBBs)*. The following information is intended to describe the appearance and handling of components shipped in desiccant packing and the materials involved. The handling information applies *only* to those devices subjected to SMT processes. Handling information covers dry component storage life, manufacturing floor life (of exposed components), rebagging information and guidelines for rebaking units if necessary.

*32-lead and 40-lead TSOP packages are the only exceptions to this practice.

Packing Materials

Moisture sensitive PSMCs packed in tubes, tape and reel or trays will be shipped in desiccant packing. Each shipping medium will contain units that have been baked dry and are enclosed in sealed Moisture Barrier Bags, (MBBs), with desiccant pouches.

- **Shipping Box.** The label on the shipping box will indicate that desiccant packed material is included (see Figure 8-3). This label will indicate the seal date of the enclosed MBB and, thereby, the remaining shelf life. Quantities of units shipped per box will also differ to accommodate the additional packing materials for shipments in tubes. For details on tube, tray and tape and reel shipments, see Transport Media Chapter, Literature Order #240822-003.

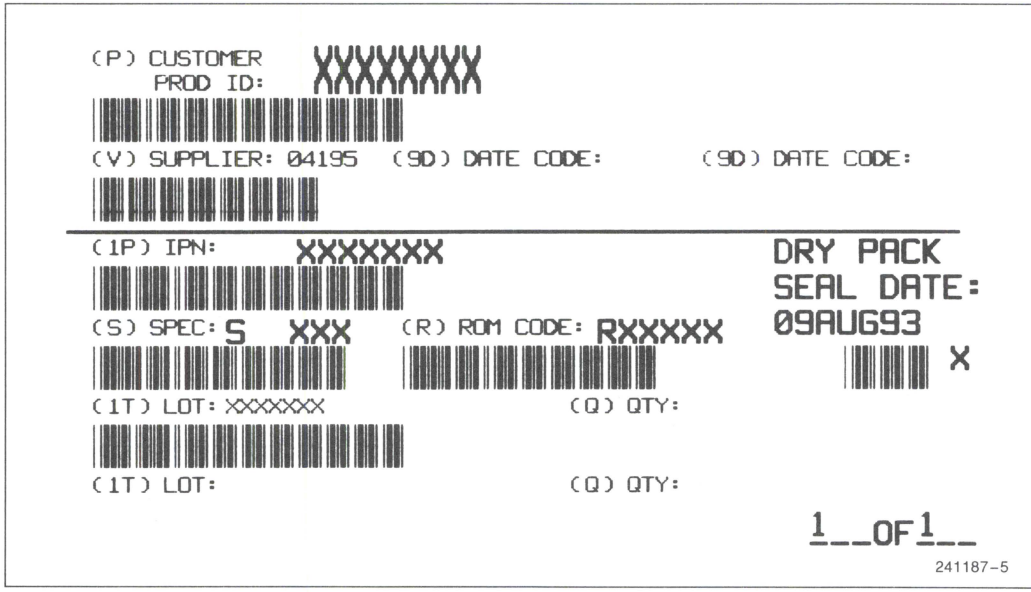


Figure 8-3. Desiccant Barcode Label

- **Moisture Barrier Bag (MBB).** Inside the shipping box is a MBB containing components. The bag is strong, ESD-safe, and allows **minimal** moisture transmission. It has been sealed at the factory and should be handled carefully to avoid any puncturing or tearing of the materials.

  A "Caution Label" (Figure -4) will be on the bag, outlining precautions that should be taken with desiccant packed units, and a Desiccant Barcode label.

  This bag is intended to protect the enclosed devices from moisture exposure and should not be opened until the devices are ready to be board mounted. The "Supporting Technical Information" section of this document provides information on technical aspects of the bag and characterization information. The "Materials" appendix, following the handling diagrams, outlines basic MBB characteristics.

- **Desiccant.** Each MBB will contain pouches of desiccant to absorb moisture that may be present in the bag. The Humidity Indicator card (Figure 8-5) should be used as the primary method to determine whether the enclosed parts have absorbed excessive moisture.

  The desiccant should not be baked and is not reusable once removed from the MBB.

- **Humidity Indicator Card (HIC).** Along with the desiccant pouches, MBB will contain a humidity indicator card (HIC). This card is a moisture indicator and is included to show the user the approximate relative humidity level within the bag. A representation of the HIC is shown in Figure 8-5. If the 20% dot on the card is *pink* and the 30% dot is *not blue*, the components have been exposed to moisture *beyond the recommended limits for use in an SMT process.* If this should happen, *in order to use these units "safely" in a surface mount application, units need to be baked dry* (see "Rebaking" section). The HIC is reversible and can be reused. Recommendations to avoid expiration of the HIC and the need to rebake units are included in the "Incoming Handling", "Shelf Life" and "Floor Life" sections.

- **Labels.** Labels relevant to this process are the Desiccant Barcode label, "Caution" label and "ID" label mentioned in the section on MBB's. The "Desiccant Barcode" label (Figure 8-3) contains the date that the bag was sealed (MM/DD/YY) and is attached to the outside of the box and on the MBB itself. The remaining storage life of the units in the bag is determined from this date. All components are guaranteed 12 months of shelf life starting from the seal date on this label (see "Storage Conditions/Shelf Life" section).

  The "Caution" label (Figure 8-4) is attached to the outside of the MBB and outlines precautions that must be taken when handling desiccant packed units if they are to be kept dry. The "ID" label is placed on the same end of the container as the desiccant barcode label.

241187-30

Figure 8-4A. "ID" Label

CAUTION

This bag Contains
MOISTURE-SENSITIVE DEVICES

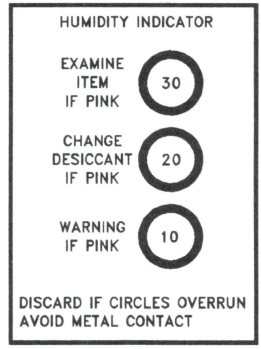
1. Shelf life in sealed bag: 12 months minimum at <40°C and <90% relative humidity (RH).
2. After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be:
   a) Mounted within 48 hours at factory conditions of ≤30°C/60% RH, or
   b) Stored at ≤20% RH.
3. Devices require baking, before mounting, if:
   a) Humidity Indicator Card is >20% when read at 23°C ± 5°C, or
   b) 2a or 2b are not met.
4. If baking is required, devices may be baked for:
   a) 192 hours at 40°C + 5°C/-0°C and <5% RH for low-temperature device containers, or
   b) 24 hours at 125°C ± 5°C for high-temperature device containers

Bag Seal Date:_____
(If Blank, see bar code label)

030140030

241187-31

Figure 8-4B. (MBB) "Caution" Label



241187-6

Figure 8-5. Humidity Indicator Card

Packing of Shipments

- **Tubes.** Units shipped in tubes will be packed with an additional precaution. Antistatic foam will be used to protect the bag from the sharp edges of the tubes and tacks. Otherwise, the units shipped in tubes will be packed with materials as indicated in Figures 8-6 through 8-10.
- **Trays.** Units shipped in injection-molded trays will also be packed with additional precaution. Antistatic foam lids will enclose the trays to protect the bag from the sharp edges of the trays. Trays will be packed with materials as indicated in Figures 8-11 through 8-13. (See "Tray Recycle Program" in Chapter 10—Transport Media and Packing 240800.)
- **Tape and Reel.** Units shipped in tape and reel are packed as indicated in Figures 8-14 through 8-16.

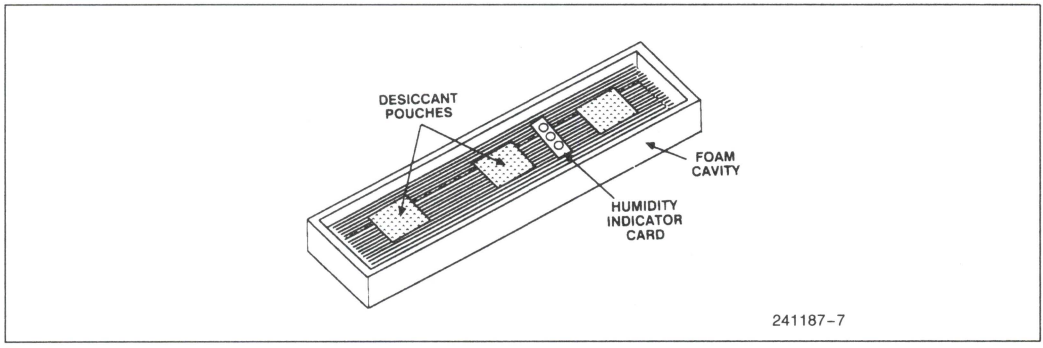


Figure 8-6. Bag Packing for PLCC Full or Half Length Tubes

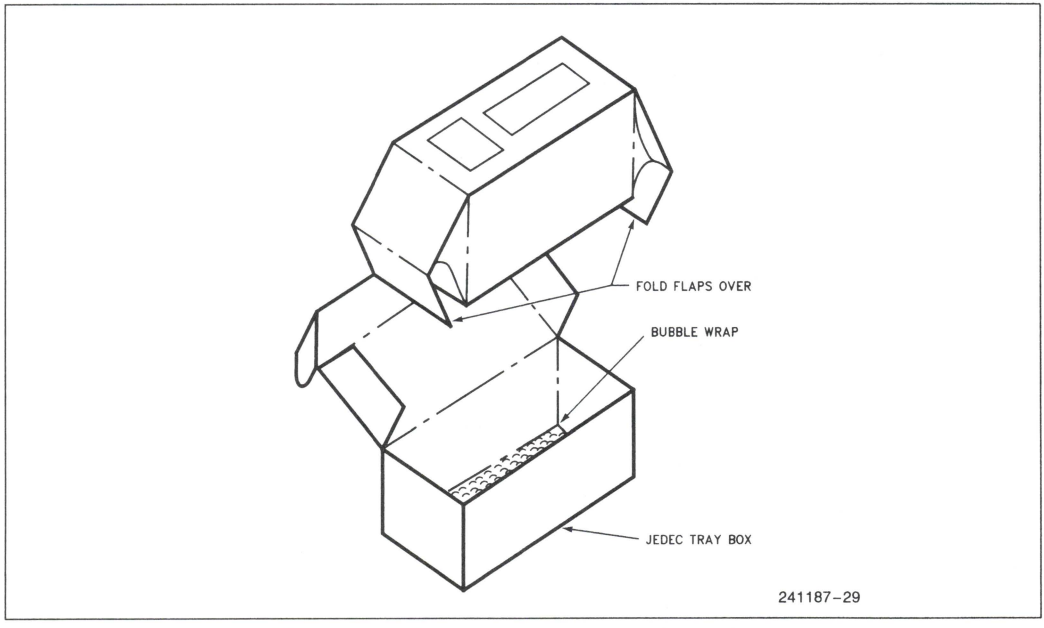


Figure 8-7. Box Packing for PLCC Tubes

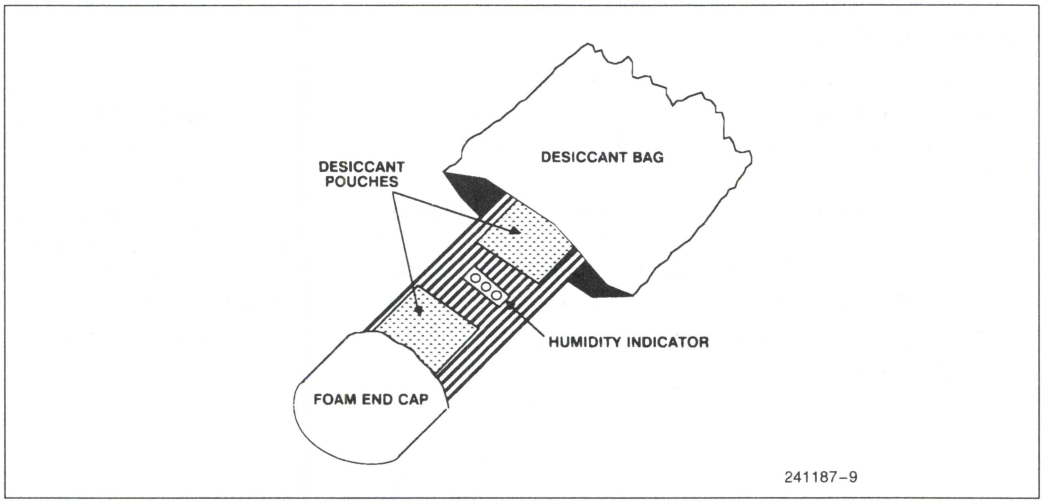


Figure 8-8. Bag Packing for PQFP Tubes

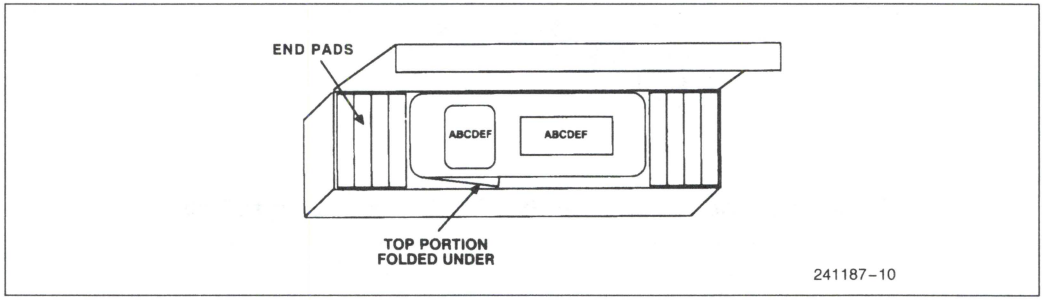


Figure 8-9. Box Packing for PQFP Tubes

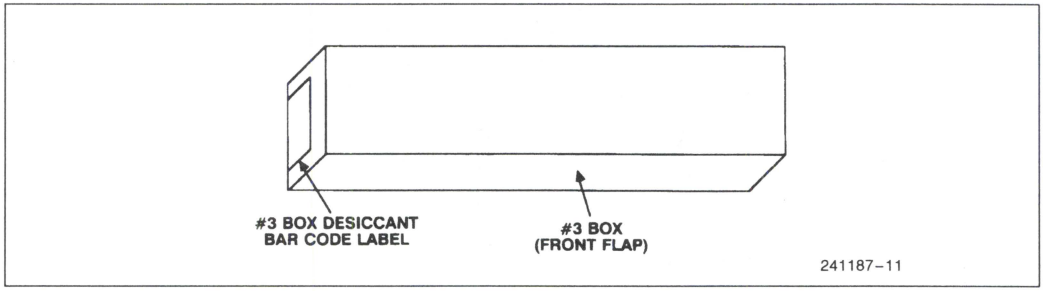


Figure 8-10. Placement of Label on Shipping Box

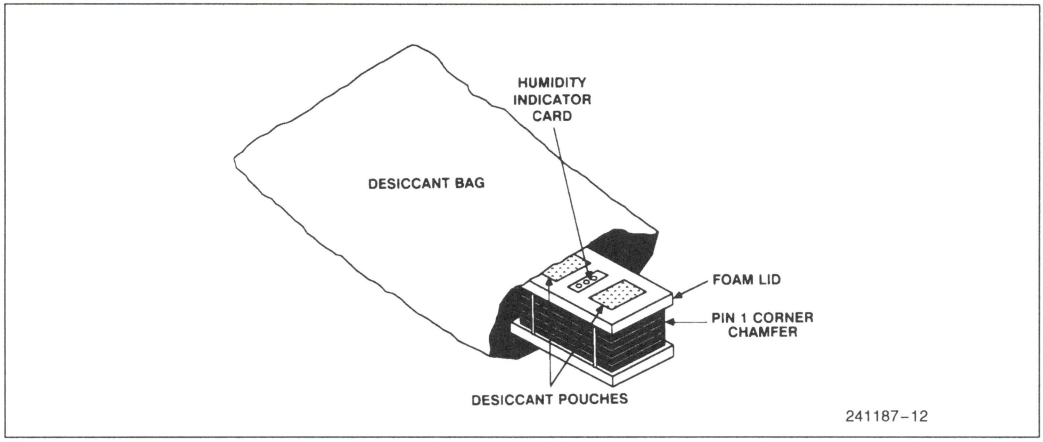


Figure 8-11. Bag Packing for Jedec Trays

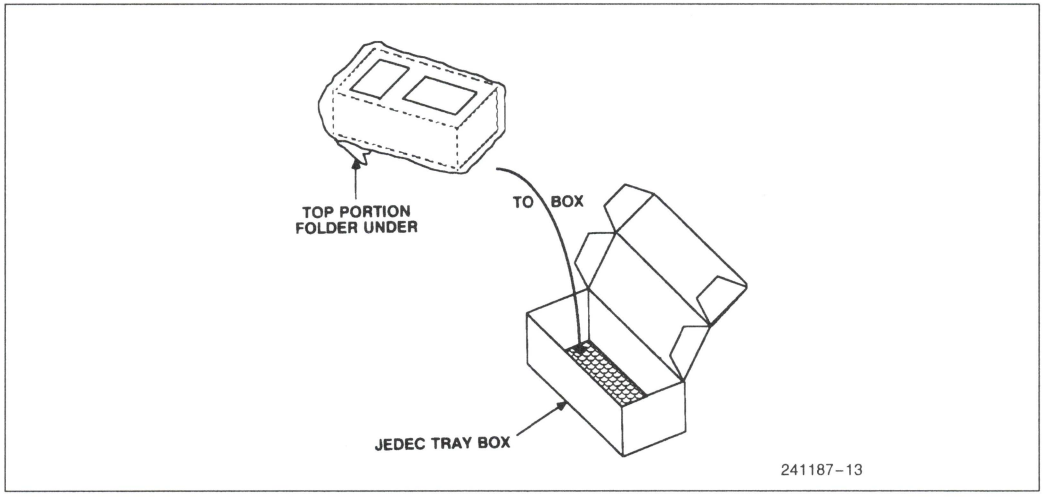


Figure 8-12. Box Packing for Jedec Trays

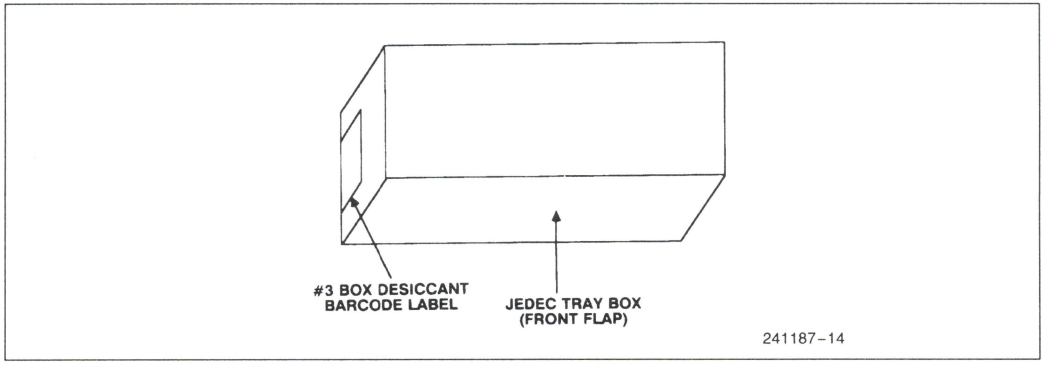


Figure 8-13. Placement of Label on Jedec Tray Box

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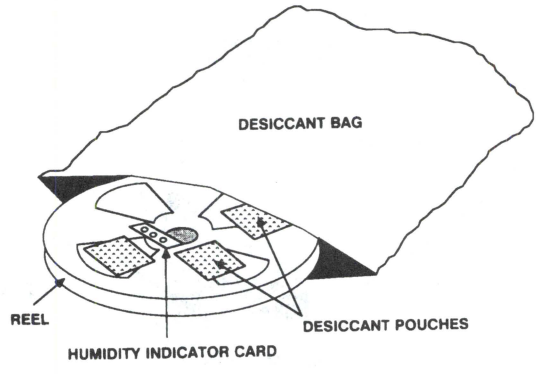


Figure 8-14. Bag Packing for Tape and Reel

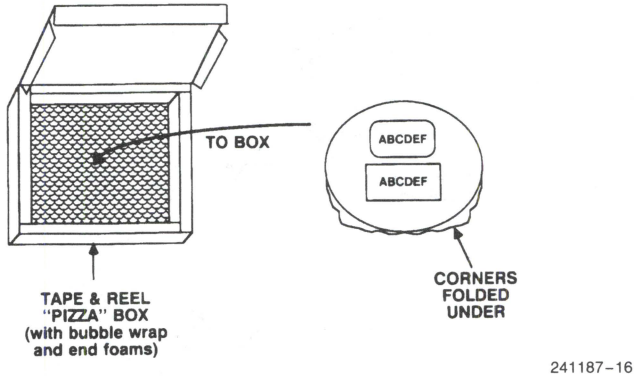


Figure 8-15. Box Packing for Tape and Reel

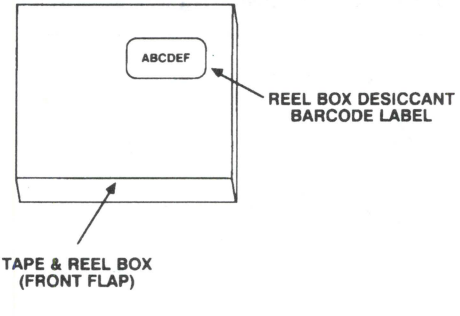


Figure 8-16. Placement of Desiccant Included Label on Tape and Reel Box

Handling

The following information details handling procedures that should be used with PSMCs packed in desiccant bags and intended for surface mount applications. Following these handling guidelines will ensure that components maintain their as-shipped, dry state alleviating package cracking and other possible moisture-related, stress-induced concerns that may be associated with the surface mount process.

- **Incoming Inspection.** Upon receipt, shipments should be inspected for a seal date within the last six months. Bag integrity should also be verified. There should not be holes, gouges, tears, or punctures of any kind that expose either the contents or an inner layer of the bag. The barcode label can be reviewed for conformance to the purchase order, but the bag should not be opened until the contents are ready to be used (either inspected or board-mounted). Please see the following "Manufacturing Conditions/Floor Life" section for details of allowable exposure times once the devices are removed from the bag or exposed to the ambient.
- **Storage Conditions/Shelf Life.** The customer will receive components in the sealed MBB between 0 and 6 months after the seal date indicated on the Desiccant Barcode label. The sealed bag and enclosed desiccant have been designed to provide a minimum of 12 months of storage (Intel storage time + customer storage time) from the seal date in an environment as extreme as 40°C and 90% relative humidity. The customer will have at *least* six months of shelf life available on the components without the need to rebake them before use.

  If the worst-case storage conditions (time, temperature, or relative humidity) are exceeded and there is a need to verify whether inventory has been affected, a bag can be opened and the HIC can be checked for expiration. If the HIC has not expired (as indicated in the "Humidity Indicator Card" section), new desiccant can be added and the bag resealed ("Resealing" section follows). If the HIC has expired, the devices should be 1) rebaked and used in manufacturing with the guidelines outlined in the "Rebaking" section, 2) rebaked and resealed in an MBB with fresh desiccant, or 3) rebaked and stored in an environment of $\leq$20%RH before they are used in a surface mount process. Please see "Rebaking" section for additional information.
- **Opening MBBs.** To open a moisture barrier bag when the contents are ready to be used or inspected, simply cut across the top of the bag as close to the seal as possible, being careful not to damage the enclosed materials. By cutting close to the seal, you will allow as much room as possible for resealing. Once the bag has been opened, please follow the guidelines for ambient exposure time in the following section to ensure that devices are maintained below the critical moisture level.

- **Manufacturing Conditions/Floor Life.** Intel, in line with the IPC revisions to IPC-SM-786 (currently in process), is classifying surface mount components into several levels of moisture sensitivity. Table 8-2 lists the 6 IPC levels of moisture sensitivity. Note that all bins are based on exposure time and environment. The latest information in the literature and from Intel studies indicates that percent weight gain moisture content is not useful for other than evaluation. Different package types/die attach area/lead count combinations will have different levels of absorbed moisture at which floor life limitations are exceeded. Therefore, Intel is recommending that units be classified by allowable exposure times. The label on the Moisture Barrier Bag lists the Moisture Sensitivity Level and the allowable floor life. See Figure 8-3.

  Once the barrier bag has been opened, Intel recommends that components be surface mounted and reflowed within the time indicated on the Moisture Barrier Bag label. This time is based on a manufacturing environment not more extreme than 30°C/60%RH. If the component can not be mounted within this timeframe, they should be put into a dry storage environment immediately, or sealed into a MBB with fresh desiccant as soon as possible. In either case, the remaining allowable ambient exposure time must be reduced by the time the units were out of the MBB or dry storage environment.

Table 8-2. Moisture Sensitivity Classification Levels for SMCs

Level	Description	Floor Life (Out of Bag) At Board Assembly Site	Moisture Exposure	
			T/RH	Time
1	Non-Moisture Sensitive	Unlimited at 30°C/85% RH	85°C/85% RH	168 hrs
2	Limited Moisture Sensitivity	1 Year at 30°C/60% RH	85°C/60% RH	168 hrs
3	Moisture Sensitive	1 Week at 30°C/60% RH	30°C/60% RH	168 hrs + MET
4	Highly Moisture Sensitive	72 Hours at 30°C/60% RH	30°C/60% RH	72 hrs + MET
5	Extremely Moisture Sensitive	48 Hours at 30°C/60% RH	30°C/60% RH	48 hrs + MET
6	Bake Before Use	6 Hours at 30°C/60% RH	Bake at 125°C for 24 Hours Before Use	

MET = "Manufacturer's Exposure Time": The compensation factor which accounts for the time after bake that the component manufacturer requires to process the components prior to bag seal, and including a factor for distribution handling.

Please contact your local Intel Sales office for specific handling questions. All of the same restrictions for exposure time (outlined above) apply. Reference ANSI/IPC-SM-786.

Where exposure times and/or ambient conditions are difficult to control, Intel highly recommends dry storage capability (please see following section).

- **In-Process Storage.** Intel *highly recommends* having dry storage capability available for units that will not be used within the allowable exposure time. PLCC's and PQFP's (≤ 100 leads) can be stored outside of the barrier bag for long periods of time if the ambient relative humidity is less than 20%. This applies to both long term and in-process storage. A desiccator with dry nitrogen or air ($\leq 5\%$RH source) is suggested for such storage. (Please see "Materials" appendix following handling diagrams for more information.) Desiccator storage conditions for larger PSMCs are currently being established.
- **Rebaking.** PSMCs need to be rebaked *if and only if* they have been exposed to excessive moisture as indicated by exceeding the recommended ambient exposure time or by expiration of the HIC (see "HIC" and "Desiccant" sections for instructions on how to determine expiration).

  In the event that the units need to be rebaked, see "Rebaking" section later in this chapter.
- **Resealing Moisture Barrier Bags.** If there is a need to reseal Moisture Barrier Bags for any reason, Intel recommends the following guidelines to ensure that the bag seal does not allow moisture into the bag. The seal area must not exhibit any separation when subject to load and temperature conditions specified in MIL-B-81705, and must be impermeable to moisture according to MIL-B-81705. Intel uses a seal pressure to 60 psi–70 psi, and a seal time of 3–4 seconds at approximately 225°C. (See "Materials" appendix following handling diagrams.) The integrity of the seal is vital to the storage life of the devices.
- **Process Flow.** Intel ships moisture sensitive PSMC which have been packed following a tightly controlled process. This flow is shown in Figure 8-17.

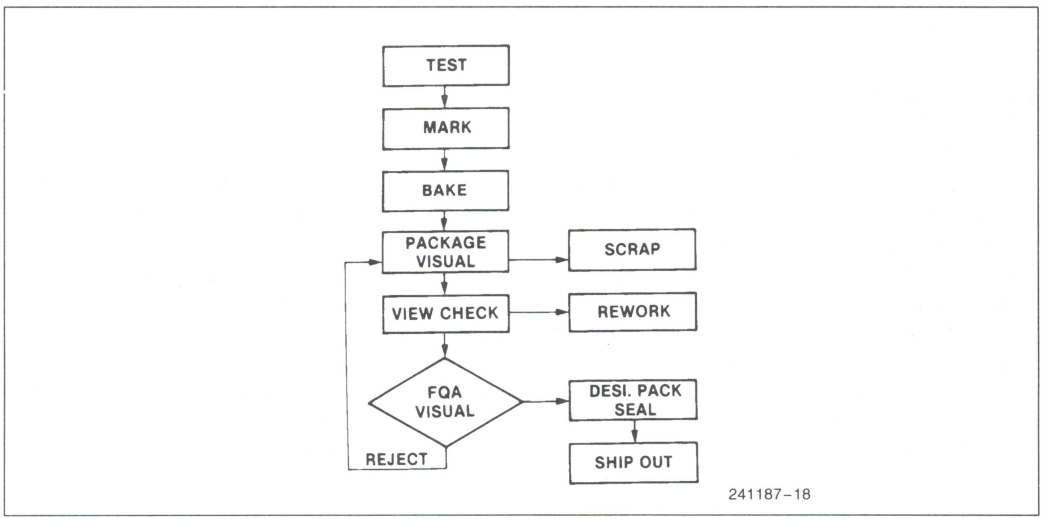


Figure 8-17. PSMC Packaging and Bagging Flow Chart

SUPPORTING TECHNICAL INFORMATION

The phenomenon of moisture induced plastic package cracking and internal delamination during high temperature reflow soldering for surface mount has been discussed by several investigators, including Intel. Moisture absorbed to a concentration dependent on the storage environment, can vaporize during the rapid heating of the solder reflow process and generate pressure at the metal leadframe-to-plastic interfaces in the package. This, along with the further stress of thermal expansion mismatches between the metal leadframe, silicon die and plastic encapsulant, can lead to delamination between the die/leadframe and the encapsulant, followed by swelling and cracking of the plastic. Subsequent high temperature exposure and moisture in the package can drive ionic contaminants through these openings to the die surface increasing the potential for device failure due to corrosion. Intel has previously published the saturated moisture level at which package cracking is observed and the moisture content for which package cracking jeopardy does not exist.

Once the cracking jeopardy of *surface mounted* PSMCs was identified, Intel characterized component absorption/desorption rates and saturation limits as a function of temperature and relative humidity. Intel engineers have proposed a model describing the kinetics of PSMC moisture absorption based on this data. The handling and shelf life guidelines outlined in the first section of this document are based upon the experimental analysis of the desiccant pack materials. The water vapor transmission rate of the moisture barrier bag (MBB), desiccant absorption rate and saturation levels, and maintainable MBB internal relative humidity were all important factors in developing the recommendations given.

Customers using PSMCs in *non-SMT* applications may continue to use PSMCs *without altering their current process flow.* Non-surface mounted PSMCs do not undergo the same temperature excursions and thermal stresses associated with the VPS or IR solder reflow processes and, therefore, do not have the same jeopardy related to them as unprotected PSMCs used in SMT applications.

Characterization Data

- **Moisture Absorption.** The moisture absorption curves for the PLCC as a function of temperature and percent relative humidity are shown in Figure 8-18. Moisture absorption characteristics of PSMCs have been used throughout this work as a worst case behavior limit because of the large die sizes involved. As shown in the curves, temperature is the controlling parameter determining absorption rate in the "short time" view. The saturation limit is a function of both relative humidity and temperature, relative humidity being, by far, the major contributor to the final weight gain of the components. Earlier work on PLCC's reported the allowable safe moisture content to be 0.11% by weight(1). This line has been overlaid on Figure 8-17. Components absorb this critical amount of moisture rapidly unless they are stored under low humidity conditions, e.g., 20%RH.

1. For PLCC and PQFP packages with ≤ 132 leads. MM-PQFP and EIAJ style QFP's have a safe allowable moisture content of 0.08%.

NOTE:
Intel has specific exposure limits on the bag label for each product.

- **Exposure Times in Different Environments.** The absorption curves for common manufacturing and warehouse environments are shown in Figure 8-19. The allowable safe moisture content line and the intersection of that line with Intel's standard manufacturing floor environment of 30°C/60%RH have been added for reference. At this condition, PLCC components absorb 0.11% moisture in 130 hours. Because Intel bakes units, then marks, packs, and ships them to customers, some of this exposure time is expended. The customer will *receive* components which have a minimum of 6 months available shelf life in the customer's warehouse and an acceptable exposure time on the customer's factory floor in manufacturing environments of ≤30°C/60%RH as listed on the bag label.

  There are options available to extend the allowable exposure time of moisture sensitive PSMCs before SMT reflow processing. Storage in desiccators on the manufacturing floor will extend the working life of units *indefinitely* as long as the time of exposure out of the desiccator is less than the specified exposure time.

More severe environments will decrease the acceptable amount of exposure time on the customer factory floor. To assess the impact of other environments, the curves of Figure 8-20 were normalized to the time that the MBB is opened on the customer floor. This family of normalized weight gain versus time curves is provided in Figure 8-20. For instance, the 30°C/60%RH curve crosses the 0.11% weight gain line at 48 hours. From these curves, exposure times in more severe factory environments can be determined. It must be noted that these figures are applicable to PLCC and PQFP packages. Thinner (or thicker) packages will have different moisture absorption/desorption characteristics and could have different moisture gain thresholds for damage.

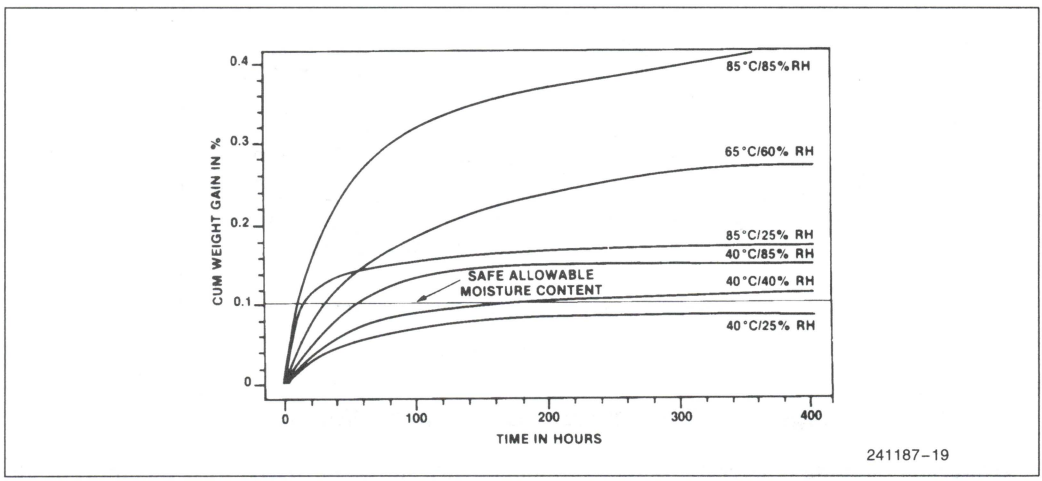


Figure 8-18. PLCC Weight Gain versus Temperature and Relative Humidity following High Temperature Bake

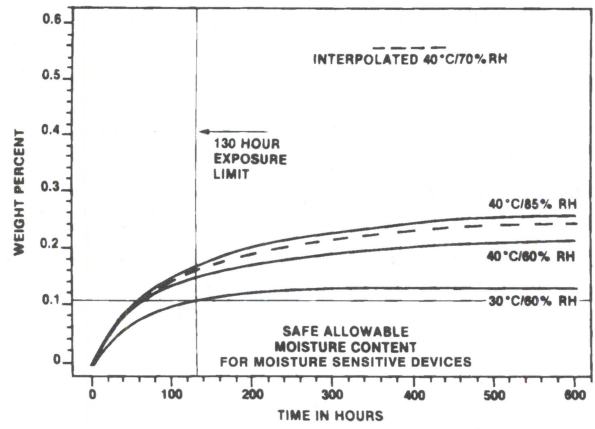


Figure 8-19. PLCC Component Weight Gain in Common Manufacturing Environments

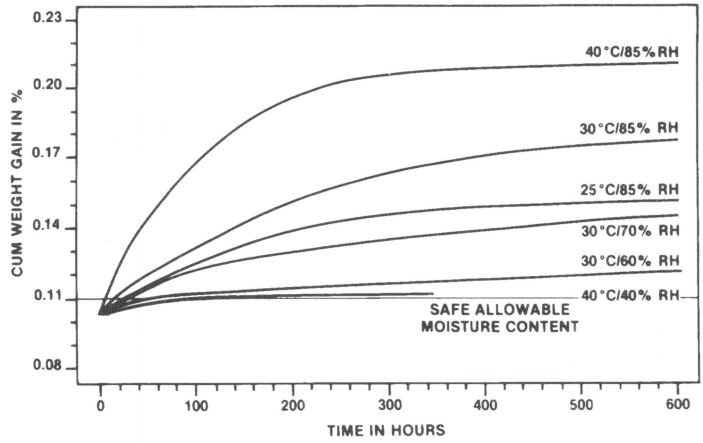


Figure 8-20. Normalized Component Weight Gain

- **Desiccant Packing (General).** When components are stored in MBBs with the appropriate amount of desiccant, it takes much longer for packages to gain the critical moisture content. After 526 hours at 65°C/60%RH, 68-lead PSMC stored in desiccant pack had absorbed 0.008% moisture. The relative humidity inside the bag during this time was $<10\%$RH as measured by the humidity indicator card. The outside storage ambient has relatively little impact on the *PSMC moisture absorption* within the desiccant packing. The respective percent weight gains of bagged components stored at 40°C/25%RH, 40°C/85%RH, and 65°C/60%RH were found to be statistically indistinguishable even after 526 hours of continuous storage. Therefore, the moisture is being absorbed preferentially by the desiccant and the PSMCs see an effective environment of $\leq 10\%$RH.

- **Desiccant.** Intel is using molecular sieve desiccant for products requiring desiccant packaging. Desiccant moisture absorption rates at 25°C/28%RH as a function of desiccant type are shown in Figure 8-21. Desiccant capacity vs. relative humidity is shown in Figure 8-22. The desiccant is supplied in 1 unit pouches. The amount of desiccant per MBB is a function of the bag surface area and water vapor transmission rate.

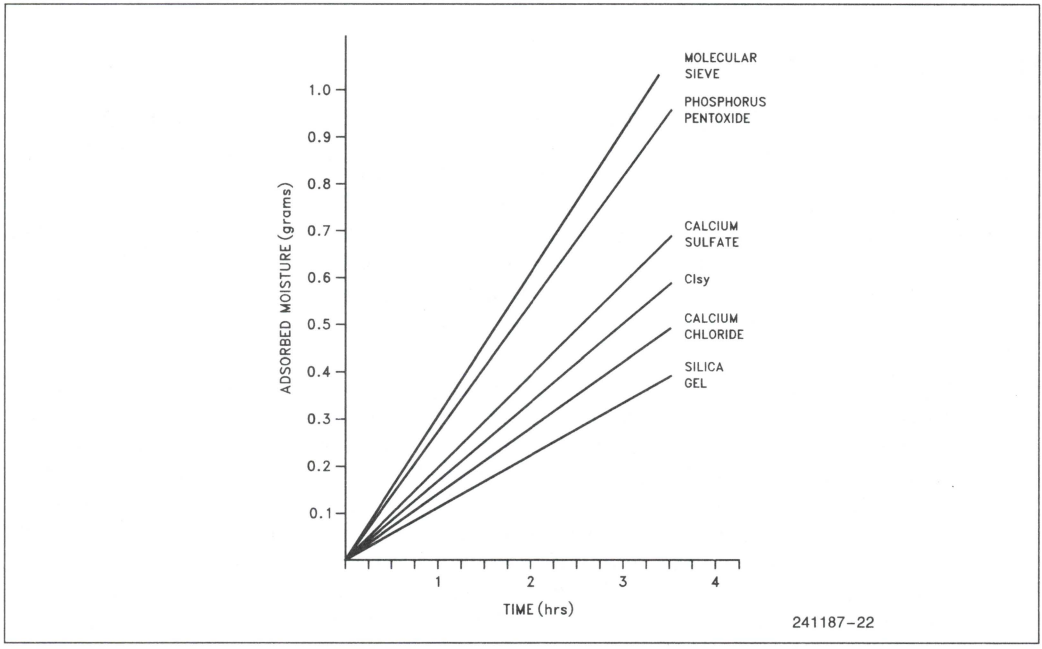


Figure 8-21. Absorption Rate 25°C/28%RH

- **Moisture Barrier Bag (MBB).** The opaque MBB is made of Tyvek and meets MIL-STD-81705 Type I for ESD, RFI, EMI and mechanical stability. The measured water vapor transmission rate (WVTR) of the bag is better than the MIL-STD requirements for moisture protection.

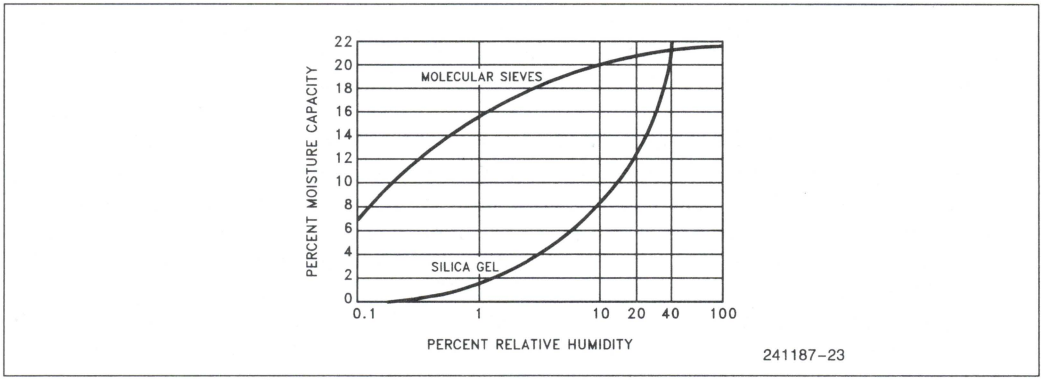


Figure 8-22. Moisture Capacity vs Relative Humidity

8

- **Amount of Desiccant.** The desiccant is supplied in 1 unit pouch. The amount of desiccant per MBB is a function of the bag surface area, 0.24 gm/in^2.
- **Shelf Life.** Intel has determined the shelf life of bagged components based upon the bag WVTR, the desiccant absorption rate, and the desiccant saturation limit. The total shelf life (Intel + customer) for bagged components in worst case warehouse conditions of 40°C/90%RH is 12 months.

Rebaking of PSMCs

- **High Temp Bake.** If the HIC indicates that the contents of the MBB have expired, the components can be baked to desorb moisture. Two bake profiles are recommended, High and Low temp. The higher temperature bake is 125°C for 24 hours (for PQFP and QFP greater than 132 leads, bake units for 48 hours at 125°C). This requires that the components be removed from plastic shipping tubes, trays or tape and reel and placed in metal or high temperature plastic containers. Components should be handled carefully to avoid lead coplanarity problems or any other type of damage. After this bake, the units may be exposed to an environment not more extreme than 30°C/60%RH for a maximum of 130 hours.
- **Low Temp Bake.** Intel has also identified a low temperature bake profile. It allows component moisture desorption in the original plastic shipping containers and, thereby, avoids possible damage to component leads that might be introduced through additional handling. The low temperature bake is a 192 hour dwell at 40°C (+5°C, −0°C)/≤5%RH. Figure 8-23 shows the curves for moisture desorption in these conditions. After 192 hours, saturated components will desorb moisture down to a residual moisture content of 0.07% worst case. This will allow a maximum of 48 hours ambient exposure time in environments not more extreme than 30°C/60%RH before the safe allowable moisture content of the package is exceeded. Refer to Figure 8-18, "Component Weight Gain in Common Manufacturing Environments", for the exposure time allowed before the weight percent moisture gain of the package reaches the critical level. The low %RH condition in the oven is critical. Longer bakes are required if the humidity exceeds 5%RH. Note that the temperature of the bake is limited by the thermal stability of the device shipping containers. The shipping containers will not hold dimension at bake temperatures higher than 45°C (40°C +5, −0 as indicated).

  It is not advisable to store PSMC units at the low bake temperature longer than the time required to dry out the units for use in the reflow. Lengthy storage times at elevated temperatures can lead to problems with intermetallic formation between the lead frame material and the lead finish, increased oxidation of the lead finish which can contribute to added reflow and wetting problems, and extended elevated temperatures can cause the antistatic properties of the shipping media (tubes/tape and reel) to deteriorate.
- **Solderability Considerations/Number of Rebakes.** Solderability tests performed on PSMCs exposed to either bake cycle are the basis for Intel's recommendations and limits on the number of allowable bake cycles. Work published in the previous technical paper (see Reference 9), established that PSMCs should not be baked more than once by the customer if using the high temperature bake of 125°C for 24 hours. Following this guideline will limit the formation of Cu_6Sn_5 intermetallic and therefore, not promote solderability degradation. The low temperature bake of 40°C for 192 hours does not require this restriction.

NOTE:
Solderability work done on solder dipped (not plated) PLCC's.

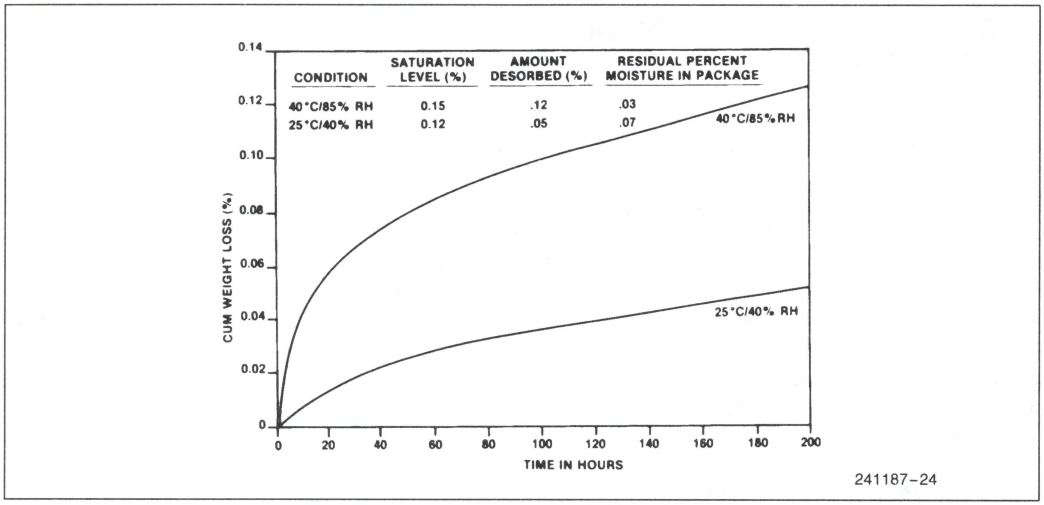


Figure 8-23. Saturated Component Weight Loss at Low Temperature

- Because components are baked in the shipping containers at the 40°C bake—tubes, trays, or tape and reel—possible outgassing products as well as intermetallic formation impact on solderability were evaluated. Figure 8-24 is a "box plot" analysis of solderability measured by coverage of the leads in "number of squares". There is overlap in the distributions of, 1) the control units stored in metal trays, 2) units stored in plastic shipping containers and, 3) units baked in plastic shipping containers, therefore, there is no statistical difference between the treatments. No difference in solderability was observed after multiple rebakes at low temperature. Based on this data, there is no restriction on the number of times devices can be rebaked at the recommended low temperature before solderability is degraded beyond acceptable limits.

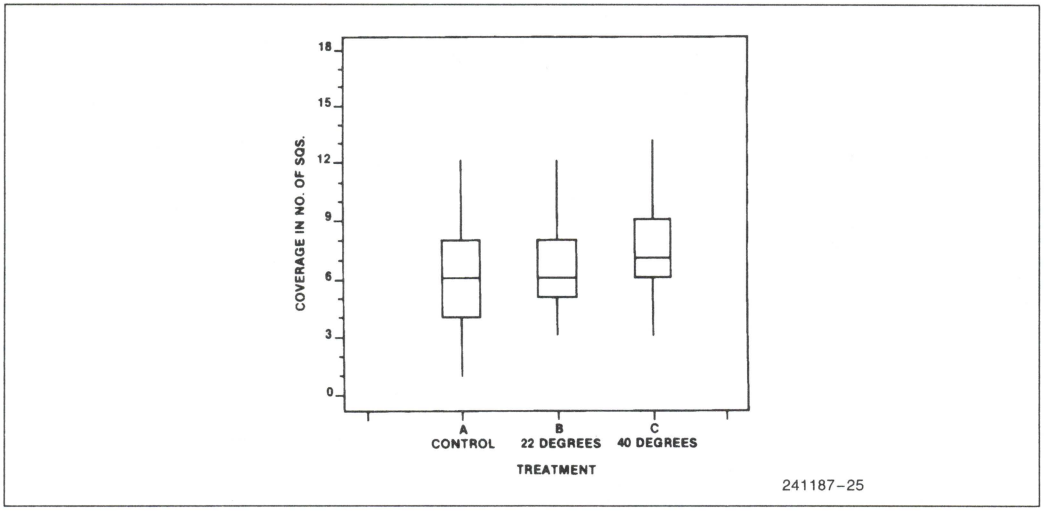


Figure 8-24. Solder Coverage versus Temperature

EVALUATION OF PSMC DEVICES FOR MOISTURE SENSITIVITY/PACKAGE CRACKING

The problem of moisture stress sensitivity and package cracking during surface mount is not unique to any one computer design or manufacturer. A method is needed for evaluating the "moisture sensitivity" of devices supplied by different manufacturers. The method that Intel has developed to determine whether a package/die combination is "moisture sensitive" with respect to package cracking follows. Uniform application of this methodology is one way to evaluate devices from different vendors to determine which devices, if allowed to absorb moisture, have a high probability of cracking during surface mount procedures. Also included is a method which can be used to assess device failure rates in surface mount applications. This can also be useful for comparison purposes and comprehends failure rates due to any kind of surface mount induced, stress-related failure. This method is commensurate with ANSI/IPC-SM-786 and IPC-TM-650 method 2.6.20.

PSMC PACKAGE CRACKING

Intel has evaluated PLCC packages for susceptibility to cracking during solder reflow processing by subjecting samples to preconditioning stresses which include moisture saturation in 85%RH/85°C for 168 hours, and solder reflow environment exposure. Package saturation in 85% RH was chosen to simulate worst case storage humidity in customers', warehouses, and 85°C is used to accelerate the moisture diffusion rate into the package. Cross sectional analysis of the package as shown in Figure 8-26, followed by optical inspection at 30X magnification was used to determine existence of package cracks. Cracking was found to emanate from the die attach pad edges and propagate either to the outside of the package or to bonding fingers of the lead frame. The results of this evaluation are described in Figure 8-25 and show that package crack susceptibility is dependent on the die attach pad dimensions and the thickness of plastic between die attach pad and nearest external surface.

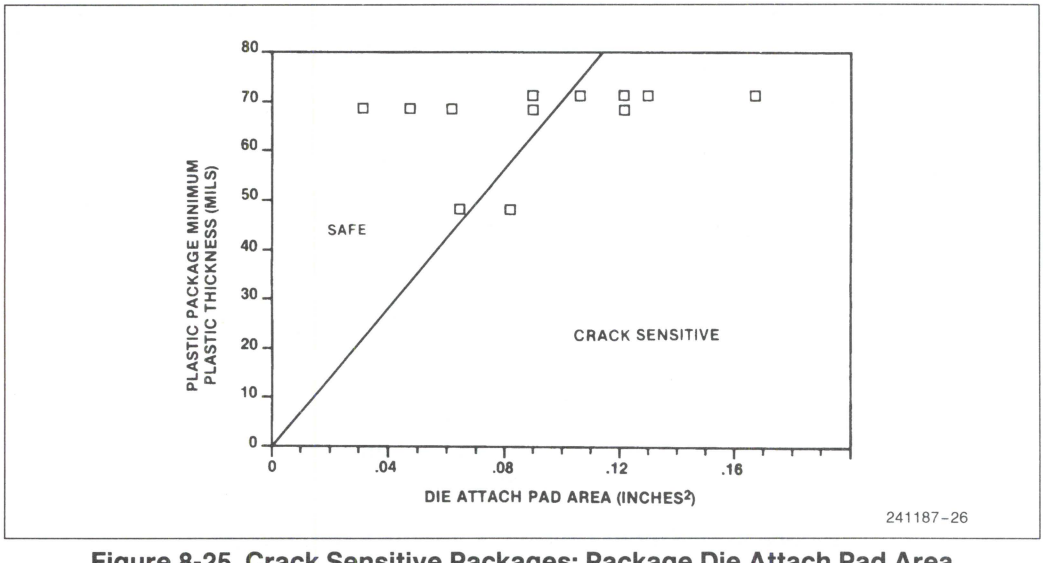


Figure 8-25. Crack Sensitive Packages: Package Die Attach Pad Area versus Package Minimum Plastic Thickness

Method for Evaluating Devices for Moisture Sensitivity

One package or product cannot be used to categorize a vendor's entire portfolio as to its moisture sensitivity. Moisture sensitivity can manifest itself in many ways, including but not limited to: bond lifts on either the die surface or die paddle, wire heal cracks, die surface thin film cracking, bond cratering, and delamination. Package design, die layout, die topography and size, and materials used in the package contribute to the overall package moisture sensitivity. Since package cracking is the severest form of moisture sensitivity, evaluation of a package for its cracking sensitivity may not uncover other moisture concerns. Package cracking sensitivity has been found to be a function of die paddle area (the area of the lead frame where the die is attached) and minimum package plastic thickness (see Figure 8-25). Each product must be evaluated individually to determine its moisture sensitivity.

- Bake 10 units of each product for 48 hours at 125°C to dry out any absorbed moisture (preferably 5 units from each of 2 date codes).
- Use acoustic microscopy to detect initial internal delamination and cracking. Record images and analyst's observations. If these parts do not meet the acceptability criteria listed below, contact vendor.
- Saturate the units by soaking in an unbiased Temperature/Humidity chamber for time and temperature/humidity combinations required for the level of moisture sensitivity being evaluated (see Table 8.2).

  Use 85°C/85%RH to simulate behavior under uncontrolled storage conditions.

  Use 85°C/60%RH or 30°C/60%RH, according to manufacturers recommendations, to simulate behavior of "dry" units shipped in desiccant pack or units baked prior to surface mount and then exposed to the ambient for the maximum allowable exposure time.

  NOTE:
  Devices which exhibit package cracking after saturation at 85°C/85%RH have an increased probability of cracking during the SMT process if they are surface mounted after storage under uncontrolled conditions. Such devices should be treated at "moisture sensitive" and only used in a "dry" state for SMT applications. This "dry" state can be achieved either by baking the units prior to surface mount or by receiving "dry" devices in desiccant pack from the vendor (as Intel currently provides).

- Run the units through three passes of vapor phase solder reflow (infrared reflow should not be used unless equivalence with VPS has been demonstrated) within 2 hours of removal from Temperature/Humidity chamber.
- Use acoustic microscopy to detect post-reflow internal delamination and cracking. Record images and analyst's observations. If these parts do not meet the acceptability criteria below, they fail the tested level.

Criteria

The general criteria defining moisture sensitivity are applied in a hierarchical manner.

1. If the components pass electrical test, there is no visual evidence of external cracks, and there is no evidence of delamination or cracks observed by acoustic microscopy, the component is considered to pass that level of moisture sensitivity.
2. If the components pass electrical test and there is backside paddle or heatspreader delamination, but there is no evidence of cracking or other delamination, the component is considered to pass that level of Moisture Sensitivity.
3. If internal cracks are observed by acoustic microscopy, components will be cross-sectioned and the cracks evaluated according to the following criteria.
   - Cracks are not allowed to intersect the bond wire, ball bond, or wedge bond.
   - Cracks are not allowed to extend from any lead finger to any other internal feature (lead finger, chip, die attach paddle).
   - Cracks are not allowed to extend more than two-thirds ($^2/_3$) of the distance from any internal feature to the outside of the package.

   Failing components must be evaluated to the next level of moisture sensitivity. Components with internal cracking that do not fail this criteria should be subjected to temperature cycle, and tested to full function electrical end points.
4. If acoustic microscopy shows any surface-breaking feature which is delaminated over its entire length, the component must be tested to the next level of moisture sensitivity. A surface-breaking feature includes: lead fingers, tie bars, heatspreader alignment features, heat slugs, etc.
5. If acoustic microscopy shows delamination which meets the following criteria the components will require further evaluation using Environmental stresses.
   - If there is any delamination on the top surface of the chip.
   - Any delamination on any wire bonding surface of the leadframe/die paddle.
   - Any delamination along any polymeric film bridging any metallic features which are designed to be isolated.

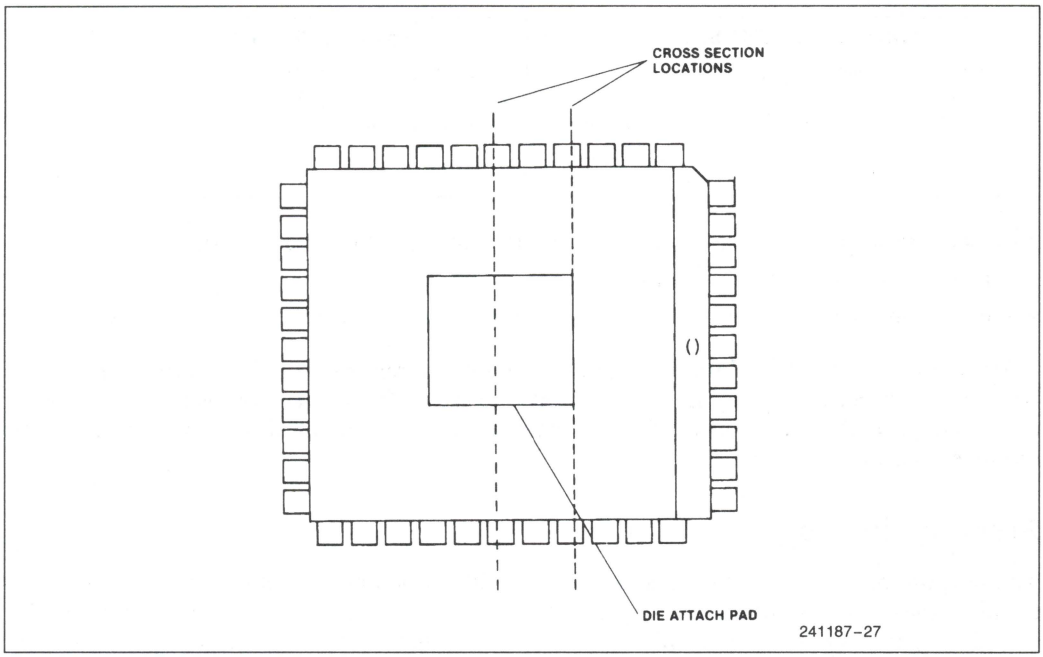


Figure 8-26. Package Crack Analysis Cross Sectioning Locations

The method outlined above indicates whether or not a device is susceptible to internal delamination or package cracking. To evaluate surface mount related failure rates over time, it is necessary to stress the units. The following describes a procedure using temperature cycling and THB (temperature/humidity, biased) stressing to evaluate failure rates due to any kind of surface mount-related, stress-induced failure.

Method for Evaluating Device Failure Rates

- Determination of failure rates and resulting comparisons should only be made after analysis of failures has been completed. Invalid failures may result and should not be used in the final failure rate assessment.
- Precondition 154 units per lot from three different lots of the same product (462 units total). This flow simulates the conditions and chemical exposures a device typically sees during board mount and rework as indicated. The component vendor should be contacted to determine the preconditioning flow and parameters appropriate for the component under evaluation.
- A reduced sample size of 90 units per lot (270) total can also be used. Sample sizes given are based on LTPD charts given in MIL-STD 38510.
- Please note that the preconditioning mentioned below is determined by the level of moisture sensitivity of the specific component.
- Following pre-conditioning, divide each of the three lots in half and subject them to the following stresses:

THB (85°C/85%RH, Biased)		Temp Cycle MIL-STD Condition "B"	
3 lots of 77 units each (45)		3 lots of 77 units each (45)	
Read-out at	168 hours	Read-out at	200 cycles
	500 hours		500 cycles
	1000 hours		1000 cycles

Numbers given in ( ) represent number of units if using reduced sample size.

- All read-outs are electrical read-outs.
- Once again, all failures should be analyzed before device failure rates are evaluated.

THB and Temp Cycle failure rates are not easily correlated to field failure rates unlike failures which occur during high temperature lifetesting (burn-in). However, failures which occur during THB and Temp Cycle stressing can indicate a potential problem and should be discussed with the vendor.

Preconditioning

The purpose of a preconditioning step in the qualification and reliability stressing flow is to simulate the actual board mounting process that the parts will see at the customer's site. By completing this stress on the units before the reliability data is gathered, the data more accurately reflects the life expectancy the units will experience in the field or customer's application.

In order to assure that SMT process stressing is comprehended in component reliability evaluations, Intel has established product qualification precondition flows to which all surface mountable plastic products are subjected prior to standard component reliability stressing*. The effect of these preconditioning stresses and their impact on long term package performance continues to be quantified. User assembly processes not comprehended by this preconditioning flow should be discussed with Intel engineers to verify package integrity of Intel PSMCs are maintained in the specific application.

*The flow is selected to match the level of moisture sensitivity classification of the specific component.

HANDLING OF PLASTIC SURFACE MOUNT COMPONENTS (PSMCs)

Maintaining the position integrity of leads on PSMC packages is a challenge. Basic precautions should be observed when handling PSMCs (such as PQFPs, QFPs, TSOPs, etc.).

Handling Precautions

NEVER TOUCH THE LEADS

Any contact with the leads of a PSMC package will likely cause coplanarity or position problems. The leads of these packages are protected (suspended) via transport media designed to ensure integrity during shipping and handling. When handling PSMCs outside their transport media (i.e., tray, tube, tape and reel) automated equipment is highly recommended.

KEEP PSMCs IN ORIGINAL TRANSPORT MEDIA

PSMCs should be kept in their original transport media until used. Manual handling of PSMCs should be avoided. Transferring PSMCs into other approved media, onto PCBs, or into sockets should be performed using automatic or semi-automatic equipment specifically designed for that purpose.

REVISION SUMMARY

The main differences between rev. -003 and -002 are the following:

- Added Moisture Sensitivity Classification Levels
- Added Method for Evaluating Devices for Moisture Sensitivity

Board Solder Reflow Process Recommendations

9

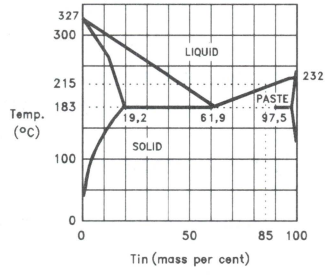
CHAPTER 9
BOARD SOLDER REFLOW PROCESS RECOMMENDATIONS

INTRODUCTION

For Intel's PLCC and PQFP packages, thermal properties are critical factors in device performance. For this reason, Intel utilizes copper alloy MF202 (98% copper, 2% tin) leadframes for optimum heat conductivity, thermal expansion and mold compound compatibility. During Intel's package assembly operation, the MF202 lead frame is plated with 85/15 ±10% tin/lead solder alloy.

In the reflow process, the solder paste must be heated above its melting point and be completely molten for the plating on the component's leads to gradually dissolve and form the desired heel and foot fillets. This mechanism is both temperature and time dependent where the reflow process is concerned.

The reflow process, particularly IR, needs to be optimized for solder paste type, component and board thermal mass and thermal sensitivity. Intel's recommendations for lead temperatures are specified in Table 9-1.



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Tin-lead phase diagram, showing the eutectic temperature of 183°C and the eutectic composition of about 62 mass % of tin; solder paste is typically 63% tin/37% lead.

Figure 9-1. Phase Diagram of Tin/Lead

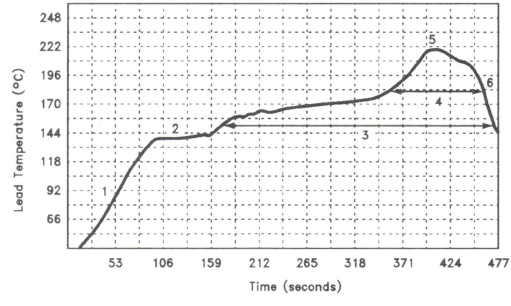

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Figure 9-2 Lead Soldering Profile in the IR Oven

9

Table 9-1. Limits for IR Reflow Profile Characteristics of Package Leads

Characteristic #	Characteristic Description	Limits
1	Initial Heating Rate of Leads	Max 4°C/Sec.
2	Peak Lead Temperature in Preheat Zone	125°C ±20°C
3	Time above 150°C	400 Secs Max
4	Time above 183°C (63/37 Tin/Lead Paste Melting Point)	Min—30 Secs. Max—150 Secs.
5	Peak Reflow Lead Temperature*	215 ±5°C
6	Cooling Rate of Leads	Max 4°C/Sec.

NOTE:
Devices classified as moisture sensitive should limit maximum body temperature to 220°C.

Reflow Profiles

SMT REFLOW EQUIPMENT

There are various types of reflow technologies. The major types are:

A: **Vapor Phase:** Uses the latent heat of condensation to reflow the solder. Has an oxygen-free atmostphere.

B: **Conduction:** Essentially a conveyorized hot-plate. Solid to solid conduction of energy.

C: **Hot Bar:** Uses a metal contact bar to apply heat directly to the leads with minimal heat transfer to the package.

D: **Infrared, Convection/infrared, and convection ovens:**

Class I: Radiant Infrared Dominant: Relies on radiant IR energy as the principle heating medium.

Class II: Convection/Infrared: Relies on combination of radiant IR energy and convection as principle heating mediums.

Class III: Convection Dominant: Relies primarily upon convection as principle heating medium.

E: **Laser:** Uses laser scanning to heat up the lead surface to reflow the solder.

Types A, B, and D are considered mass reflow processes. Method D represents the vast majority of reflow operations.

METHODS OF MEASURING PROFILES

Profile measurement is an exacting art that must be continually monitored. Usually there is no "one profile does all." Special care must be taken to insure that the proper placement for the thermocouples is achieved to accurately measure the desired surface temperature.

There are at least three points that must be measured on a board during the reflow profiling. These are the actual board temperature at the hottest point on the board, the lead surface temperature, and the package body temperature of the larger I.C. components. The lead temperature measurements are usually taken by placing the thermocouple on the surface of the lead. The package body temperature is taken by attaching the thermocouple on the top of the package body of the largest component on the board. The reflow temperatures for IR and VPS processes are listed in the tables.

VPS REFLOW PROFILE

A typical vapor phase reflow profile of a SMT solder joint in a batch oven is shown in Figure 9-3. Table 9-2 lists the important characteristics and parameters for a VPS process. The actual board and lead surface temperatures may vary slightly. To establish a vapor phase profile for batch machines, the elevator speed and board dwell time in the primary zone have to be established.

IR/CONVECTION REFLOW PROFILE

A typical reflow profile of a IR/Convection reflow operation is listed in Figure 9-2 and the important parameters are detailed in Table 9-1. To establish an infrared reflow profile, the conveyor speed and the oven panel/emitter temperatures have to be established. These will be dependent on the type and size of board used, the amount of components on that board, the type of flux and paste being used, the size of the components being reflowed, the recovery time of the oven, and the loading pattern on the belt.

HEATING RATE

To avoid a thermal shock on sensitive components, their maximum heating rate, also called the maximum ramp rate of the temperature, should be controlled. In Figure 9-2, the maximum ramp rate occurs in preheat zone of the IR oven.

*Maintain plastic body temperature of PSMC's below 220°C to avoid package cracking and other thermally induced failures.

For vapor phase reflow, with proper elevator or conveyor speed and preheat temperature adjustment, the maximum heating rate can be controlled below 6°C per second.

PEAK TEMPERATURE IN PREHEAT ZONE

The boards are preheated during reflow process. To avoid over-baking the solder paste and exceeding the glass transition temperature of the epoxy in FR-4 boards, the peak temperature in the preheat zone of the boards and the solder paste on the lands should be 125°C ±20°C. (See Table 9-1)

Table 9-2. Limits for VPS Reflow Profile Characteristics

Characteristic #	Characteristic Description	Vapor Phase
1	Maximum Heating Rate	6°C/sec
2	Peak Temperature in Preheat Zone	125°C
3	Duration of Time above Melting Point of Solder	Min—10 secs Max—80 secs
4	Peak Reflow Temperature	215 ±5°C

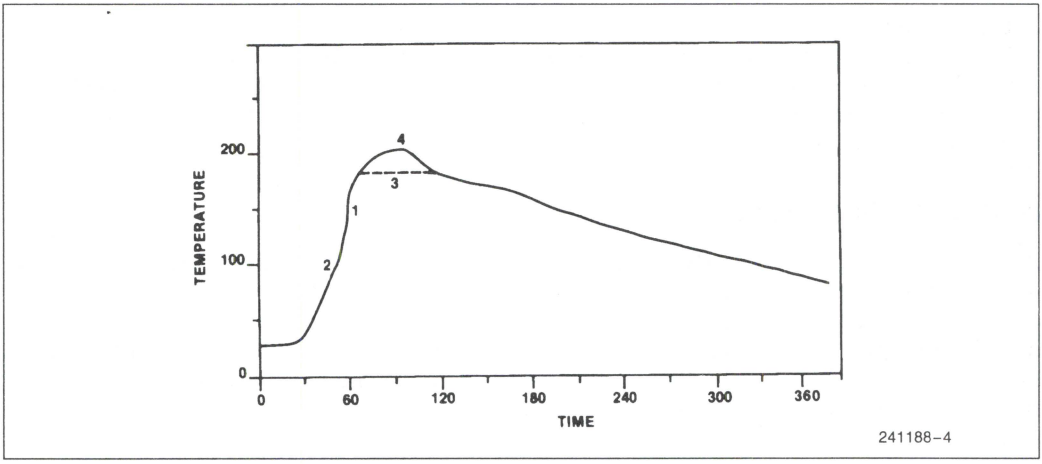

Figure 9-3. A Typical Vapor Phase Reflow Profile for an SMT Solder Joint in a Batch Vapor Phase Machine

Time Above 150°C

The time when the board temperature is above 150°C should be minimized. Glass epoxy FR-4 boards can be damaged if kept above 150°C for an extended period of time because the glass transition temperature of the epoxy is exceeded. This time should be 400 seconds maximum. (See Table 9-1)

TIME ABOVE SOLDER MELTING POINT (183°C)

A minimum of 30 seconds and maximum of 150 seconds (see Table 9-1) is recommended for the duration of time that the solder at the joint is above its melting point. The solder should be given sufficient time to flow and wet the lands and the leads. Extended duration above the solder melting temperature may damage the board and sensitive components. In addition, excessive intermetallic compound formation between the solder and the base metal of the lands and leads will occur. This may degrade solderability and solder joint fatigue characteristics.

PEAK REFLOW TEMPERATURES

The peak temperature of the solder joint during reflow should be high enough for adequate flux action and solder flow to obtain good wetting. However, it should not be so high as to cause component and board damage or discoloration. In infrared reflow ovens, the peak reflow temperature is primarily controlled by the panel temperatures in the reflow zone and secondarily by the conveyor speed. For moisture sensitive devices the Package body temperature should not exceed 220°C. Package body temperature can be measured with a thermocouple attached to the center of the top surface of the package. In infrared reflow ovens, the peak temperature of the SMT Lead is in the range of 215 $\pm$5°C. In vapor phase reflow, the peak reflow temperature of the solder joint is determined by the boiling temperature of the primary fluid and the dwell time of the board in the primary zone. For both reflow processes, the peak reflow temperature of the SMT package body should not exceed 220°C. (See Table 9-1)

COOLING RATE

Cooling rate: The cooling rate of the solder joint after reflow is important because the faster the cooling rate the smaller grain size of the solder. Smaller grain size solder has a higher fatigue resistance. If fans are used to cool the boards after they exit the oven, a cooling rate of up to 6°C per second at the solder freezing point can be easily achieved.

NITROGEN ATMOSPHERE

Nitrogen atmosphere furnaces are being used with the no clean fluxes. It should be noted, that the solder paste manufacturers are developing a solder paste that will achieve "no clean" results in a normal atmosphere.

TROUBLE SHOOTING

The table shown below (Table 9-3) outlines potential board solder problems.

Table 9-3. Board Soldering Diagnostics

Observation	Explanation	Probable Cause(s)
1. Insufficient or no Solder Fillet	Poor Fusing between Solder Paste and Plated Lead	1. Uneven Land and Lead Temperatures 2. Lead Coplanarity 3. Component Foot Angle 4. Insufficient Solder Paste 5. Peak Reflow Lead Temperature Too Low* 6. Poor Solderability of Leads
2. Bridges and Icicles	Solder Connecting or Partially Connecting Adjacent Leads or Lands	1. Excessive Solder Paste 2. Excessive Component Placement Pressure 3. Solder Paste Misplacement 4. Solder Paste Integrity 5. Bent Leads 6. Board Vibrations during Soldering
3. Dewetting	Solder Does Not Adhere to Lead or Land	1. Poor Solderability of Lands 2. Poor Solderability of Leads 3. Solder Paste Integrity
4. Solder Balls	Solder Agglomerates on Land	1. Solder Paste Misplacement 2. Solder Paste Integrity
5. Exposed Copper at Lead Tip	Poor or No Fillet Formation at Toe	1. Lead Trimmed after Plating; Exposed Copper at Lead Tip by Design (No Reliability Issue)

*Caution: Leads of larger packages heat slower.

Rework Profiles

The three methods for reworking fine pitch packages (<50 mils) are: 1) manual rework with a soldering iron, 2) blow hot air on the package leads and remove the package when the solder melts, and 3) use focused InfraRed (IR) energy to heat the package leads and remove it when the solder melts.

Manually reworking a package by a skilled rework operator has the least likelihood of damaging the printed circuit board. This method entails clipping all the leads of the defective package manually and removing the package. The leads, still attached to the lands, are then removed by melting the solder with a small tip, low wattage, soldering iron. The remaining solder on the lands is removed using solder wick. Putting a new package on the board is the most difficult part of the process. The best way to do this is to manually align the package on the lands with the aid of a microscope, then solder a couple of leads to the lands to keep the package from shifting during the ensuing rework. The leads of the package are soldered one at a time.

This method requires the highest skill.

Hot air removal is by far the most widely used method of removing fine pitch packages. Hot air is directed onto the leads of the defective package until the solder melts and the package is lifted off by vacuum (either a wand or nozzle) or with tweezers. The lands on the board are cleaned up with solder wick. Solder paste is reapplied (see Figure 2). Hot air is then applied again to the solder leads to reflow the solder paste.

Focused IR is a fairly new rework process but works similar to hot air. An IR lamp is used with a template that focuses the light on the defective package leads until the solder melts. The package is then lifted off by a vacuum wand or tweezers. The IR rework method is preferred since the heat is directed onto the leads and the package body stays cooler.

Table 9.4. Pros and Cons of Three Rework Methods

	Pros	Cons
Manual Rework	Inexpensive Rework Equipment Minimum Package and Circuit Damage	High Skill Needed Process Good to 20 mil Pitch Tedious and Time Consuming
Hot Air Rework	Repeatable Process Less Time Consuming Process Good to 16 mils Pitch	Center of Package is Hotter than the Leads May Burn and Warp Circuit Board Expensive Equipment
Focused IR Rework	Center of Package Stays Cooler than the Leads Repeatable Process Less Time Consuming Process Good to 15 mils Pitch	Expensive Equipment May Burn and Warp Circuit Board

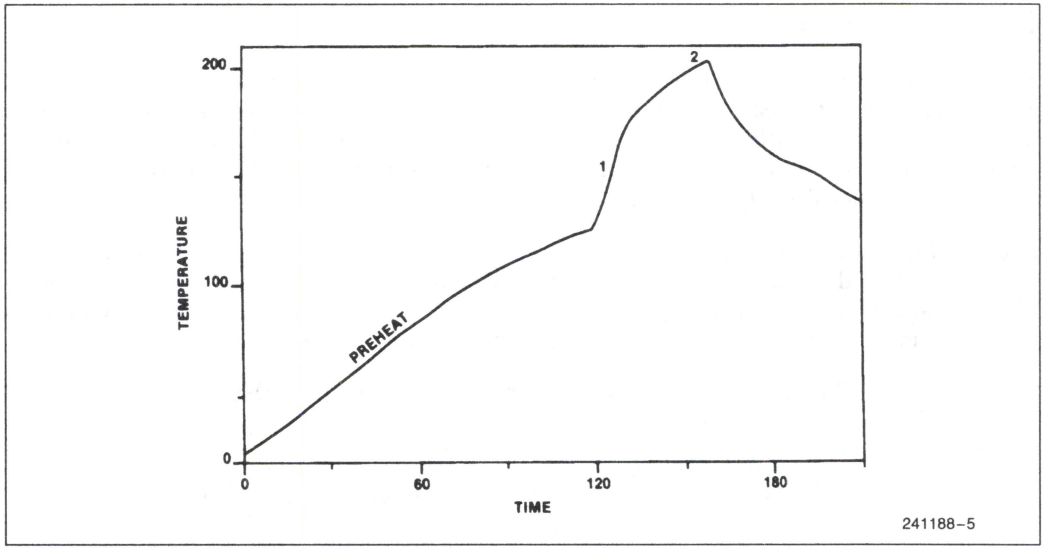

Figure 9-4. A Typical Temperature-Time Profile of a SMT Package While the Package was Being Reworked With a Hot Air Rework Machine

PEAK TEMPERATURE

The peak temperature of the leads during the rework procedure should obviously be greater than the melting point of the solder in the solder joint. However, if the peak temperature is too high there is the possibility to damage the package or the printed board by excessive heat application. For eutectic tin-lead solder, this peak temperature, denoted as (2) Figure 9-4, should be 220°C. Ensure that the package body temperature is kept at 220°C or less.

SMC BOARD REMOVAL TECHNIQUES

Intel recognizes the need for SMC board removal procedures that maintain the electrical and mechanical integrity of the component leads. The requirement for electrical testability of removed SMCs is driven by the need (1) to confirm device failure as the cause of board-level nonfunctionality, (2) correlate device failure between the customer board assembly site and Intel, and (3) perform electrical testing as part of the failure analysis procedure. Therefore, the following removal procedure has been developed to ensure component lead coplanarity and lead finish integrity.

Recommended Materials for Removal of SMCs

Materials used in the removal of SMCs are as follows:

- PCB with device to be removed
- Pace Craft-100, Air-Vac DRS-21, or equivalent* hot air solder reflow system
- Nozzle for optimized air flow. The nozzle is package dependent.
- Vacuum cup. The vacuum cup should be large enough to cover the center of the device without extending over the leads.
- Tweezers
- Safety glasses
- Pallet to retrieve component once it is removed
- Solder wick or hot air gun/blade

NOTE:
*The above is not an endorsement of any kind nor a warranty of performance of the equipment or company.

BOARD PREPARATION

Many plastic surface mount components and some ceramic chip components are moisture-sensitive. In addition, glass fiber-reinforced PCB materials can be subject to measling and other thermal-/humidity-induced damage.

As discussed in the section on desiccant pack, the package body is not heated by direct impingement of hot air. However, it can reach significant temperatures by radiant and convective heating from proximity to the reflow air nozzle. Therefore, rework procedures should be calibrated to prevent package body temperature from exceeding 220°C. Either hot air or focused IR rework equipment may be used. Focused IR is preferred because plastic package body stays cooler than the package leads.

Moisture-sensitive surface mount components should be dried by a prebake prior to rework to prevent damage to the board and the component. If it is determined that the component for removal is not moisture-sensitive, standard assembly handling and preheat procedures should be followed (see section below on "Removal Procedures"). If the component has been exposed to excessive moisture, it is necessary to dry it by baking the entire assembly at either 125°C for 24 hours or 40°C for 192 hours.

The air flow of the rework nozzle should be calibrated to ensure that leads and solder exceed the reflow temperature of the solder joint. The temperature of the package body should remain below 200°C.

REMOVAL PROCEDURES

The following procedures are recommended for removing SMCs from the PC board; using a hot bar system:

- Turn on the rework equipment at least 20 minutes before beginning the removal procedure to ensure that the air flow is at the correct temperature. Insert the PCB into the work holder.
- Adjust the work holder so that the device is centered under the hot gas nozzle. Lower the nozzle over the device and align. The alignment of the nozzle to the device is critical to ensure a uniform heating rate of the leads.
- Raise the nozzle and lock it into position. Lower the vacuum cup and check that it is the proper size.
- To reflow the solder, set the timer for the appropriate dwell time for the package type and size, as listed in Table 9-5. Pressure and time can be adjusted to optimize the process, but any modifications for increased throughput should not increase the temperature of the component body above 220°C.

  Lower the nozzle until it is 5 mils–10 mils above the shoulder of the leads. This height is crucial: If the nozzle is too high, the heating time must be increased; if positioned too low, the nozzle can cause damage to the leads.
- Using the automatic mode, reflow the solder. Once the air flow has shut off, immediately raise the component from the board. Icicling can be minimized or eliminated by removing the component from the board surface quickly using a smooth upward motion. The direction of removal must be normal to the plane of the board to prevent bridging. Do not twist or tilt the component during the removal process.
- To retrieve the component once it has been removed from the board, use the pallet (Pace safety handle). Turn off the vacuum and let the part drop onto the pallet. The drop distance should not exceed 2 in.

NOTE:

If resistance is felt when lifting the component off the board surface, do not force the part. Re-expose the unit to the heating cycle and then repeat the removal process. If the component still will not separate from the board, terminate the removal procedure. Determine if the component has been adhesively attached to the board. If so, alternate removal procedures—not covered here—will be required for removal.

Table 9-5. Parameters for Component Removal (Based on the Pace Craft-100)

Package Type	Lead Count	T_{lead} Center (°C)	T_{lead} Edge (°C)	Min Time (sec)
PLCC	32	282	277	25 +5/−0
	44	291	281	25 +5/−0
	68	277	276	35 +5/−0
PQFP	100	270	250	35 +5/−0
	132	280	250	35 +5/−0
	164	280	250	35 +5/−0
Cerquad	32	269	271	55 +5/−0
	44	289	277	55 +5/−0
	68	251	252	60 +5/−0

NOTES:
Pace air stream temperature = 350°C
Pace N_2 pressure = 40 psi

REWORK OF LEAD SURFACE MORPHOLOGY AFTER REMOVAL

Intel has found that careful removal of SMCs using the above recommended procedures greatly reduces the need to rework leads. However, if bridging or icicling occurs, Intel recommends the use of solder wick or a hot air gun for rework.

Bridging can be removed by using a solder wick. Holding the solder wick over the bridged leads, bring a fine-tip soldering pencil in contact with the bridged area. When the solder reflows, touch the wick to the molten solder, absorbing the excess.

Icicling can be eliminated by reflowing the solder with a hot air gun ($T > 190°C$). Place the part, leads up, on a heat-resistant horizontal surface. Run the hot air blade or gun across the affected leads, reflowing the solder. Allow the solder to fully resolidify before moving the component. Be sure that the hot air knife does not increase the localized package body temperature above 200°C.

NOTE:

This procedure was developed on a Pace Craft-100 rework station. Critical configuration requirements include a hot air source capable of maintaining 350°C, a nozzle design that evenly distributes air flow to all four sides of the package, and a timer. *Intel recommends that customers calibrate their removal systems to achieve commensurate parameters.* Calibrate the component lead temperature, time to reflow, and capability for component removal normal to the plane of the PCB to correlate to this set of recommendations.

SUMMARY

Intel recommends that three critical parameters be met to ensure electrical testability of a component* removed from printed circuit boards: (1) The solder must be completely molten before removal is initiated; (2) the removal direction must be normal to the plane of the board; and (3) no movement, in-plane or tilting, of the removed component should occur until the solder completely resolidifies. Intel recommends specific temperatures and dwell time at temperature as a function of package type and size.

NOTE:

*This pertains to components that have not been adhesively attached to the board for double-sided board usage.

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11. Intel Package Connections, Spring 1992.
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REVISION SUMMARY

- Changed Peak Reflow Temperature

Transport Media and Packing

10

CHAPTER 10
TRANSPORT MEDIA AND PACKING

TRANSPORT MEDIA

Tubes

Plastic shipping and handling tubes are manufactured from polyvinyl chloride (PVC) with an antistatic surfactant treatment. Standard tubes for most package types are translucent and allow visual inspection of units within the tube. Carbon-impregnated, black conductive tubes are available for all parts, where required by device or use characteristics.

Tube profiles are designed with minimum clearance over the maximum package dimensions to reduce damaging movement of the device within the tube. For some package types, tubes have "riding rails" on which the packages rest while in the tube. The rails protect the fragile leads from touching anything in the tube. Nylon tacks, or rubber plugs are used to retain the units. All tube wall thicknesses are 0.025 in. to 0.040 in. Tables 10-1 through 10-8 show tube dimensions, cross-sections, and quantity per tube for most Intel package types. Further information on new packages should be requested through Intel Field Sales.

Table 10-1. PLCC Shipping Tube Dimensions (In Inches)

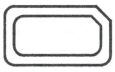
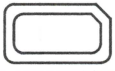
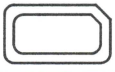
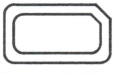
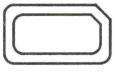
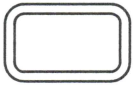
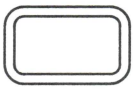
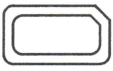
Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
20L Square		0.030	19.375	0.480	0.263	46
28L Square		0.030	19.375	0.580	0.263	37
44L Square		0.025	19.375	0.780	0.250	26
52L Square		0.030	19.375	0.880	0.263	23
68L Square		0.025	19.375	1.090	0.250	18
28L Rectangular		0.025	19.375	0.480	0.220	30
32L Rectangular		0.025	19.375	0.580	0.220	30
84L Square		0.040	19.375	1.300	0.288	15

Table 10-2. Cerquad Shipping Tube Dimensions (In Inches)

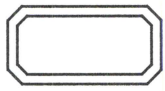
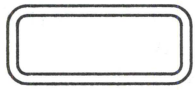
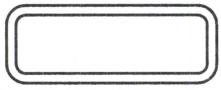
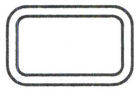
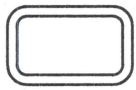
Lead Type	Cross Section (W x H)	Wall Thickness	Inside Dimensions			Quantity Per Tube
			Height (H)	Width (W)	Length (L)	
44SQ		0.025	0.200	0.730	11.50	11
52SQ		0.025	0.200	0.820	11.50	11
68SQ		0.030	0.200	1.040	11.50	9
28SQ		0.030	0.200	0.520	11.50	15
32SQ		0.030	0.175	0.530	11.50	12

Table 10-3. PQFP Shipping Tube Dimensions (In Inches)

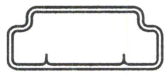
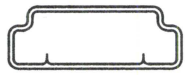
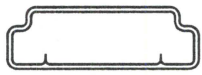
Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
84L PQFP		0.030	9.50	0.999	0.280	10
100L PQFP		0.030	10.50	1.099	0.280	10
132L PQFP		0.030	12.50	1.299	0.280	10

Table 10-4. LCC Shipping Tube Dimensions (In Inches)

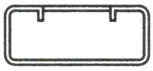
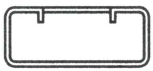
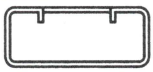
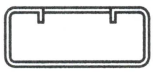
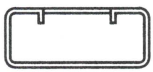
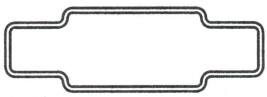
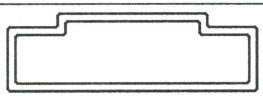
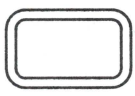
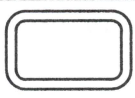
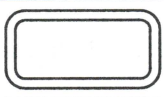
Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
18L		0.025	11.5	0.370	0.165	25
20L		0.025	11.5	0.370	0.165	25
28L		0.025	11.5	0.530	0.165	22
32L		0.025	11.5	0.535	0.207	18
44L		0.025	11.5	0.736	0.180	16
68L Type "A"		0.025	11.5	1.060	0.235	10
68L Type "B"		0.025	11.5	1.060	0.260	10
32L J-Lead Rectangular		0.030	11.5	0.590	0.235	16
32L J-Lead Rectangular EPROM		0.030	11.5	0.600	0.260	16
44L J-Lead Square		0.025	11.5	0.786	0.250	15

Table 10-5. PGA Shipping Tube Dimensions (In Inches)

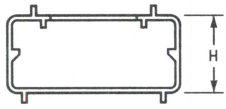
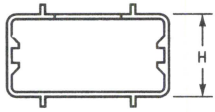
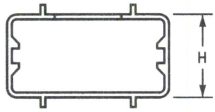
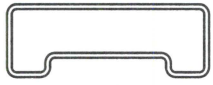
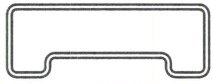
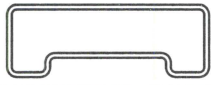
Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
68L		0.040	20	1.255	0.460	15
88L		0.050	20	1.470	0.720	12
132L		0.045	20	1.565	0.720	11

Table 10-6. Flatpack Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
18L* Ceramic		0.020	20	0.810	0.290	18
68L Plastic		0.040	20	2.138	0.628	9
68L Ceramic Quadpack		0.035	20	2.120	0.610	9

*Aluminum Tube

Table 10-7. PSOP Shipping Tube Dimensions (In Inches)

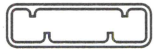
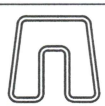
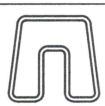
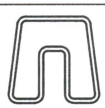
Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
44L		0.030	20	0.787	0.213	17

Table 10-8. DIP Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
16L		0.020	20	0.600	0.510	24 (P) 23 (D) 23 (C)
18L		0.020	20	0.600	0.510	20 (P) 21 (D), (C)
20L		0.020	20	0.600	0.510	18 (P), (D) 17 (C)
24L (300 mil)		0.020	20	0.600	0.510	15
28L (300 mil)		0.020	20	0.600	0.510	14 (P) 13 (D)
22L (400 mil)		0.030	20	0.727	0.535	17
24L (600 mil)		0.022	20	0.890	0.495	15
28L (600 mil)		0.022	20	0.890	0.495	13
32L		0.022	20	0.890	0.495	11
40L		0.022	20	0.890	0.495	9
48L		0.022	20	0.890	0.495	7 (P) 8 (C)

NOTE:
(P) = PDIP
(C) = Ceramic Sidebrazed
(D) = CERDIP

Carriers

Additional protection from lead damage is necessary for the fragile leads of the flatpack packages, which are shipped flat to be trimmed and formed at the customer site. Plastic carriers are used to hold each unit, then the loaded carrier is placed in the tube. Carriers are either coated with antistatic surface treatment or are intrinically static dissapative. Figures 10-1 through 10-3 show a variety of carrier types.

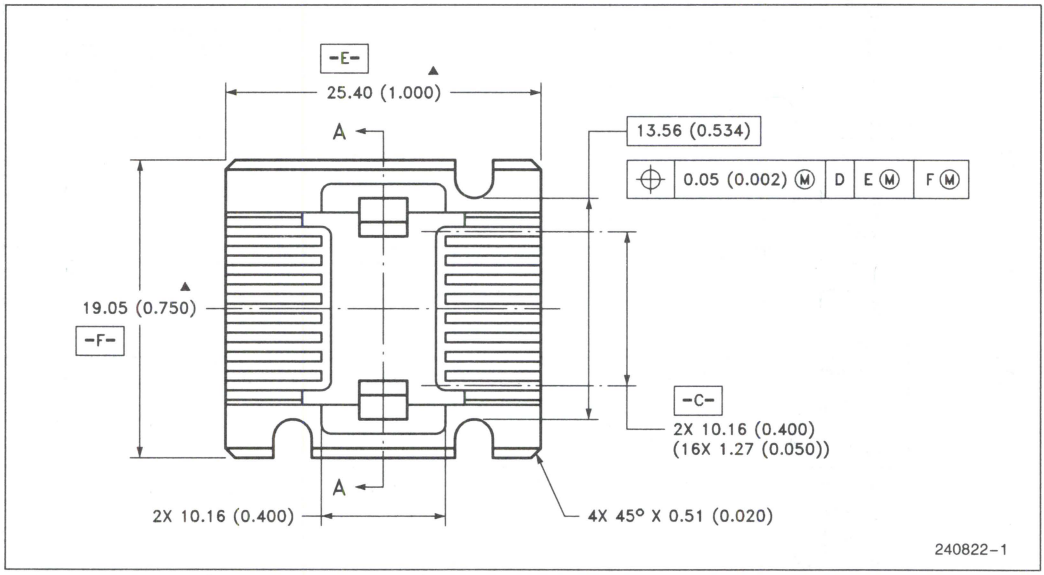


Figure 10-1. 18-Lead Ceramic Flatpack Carrier

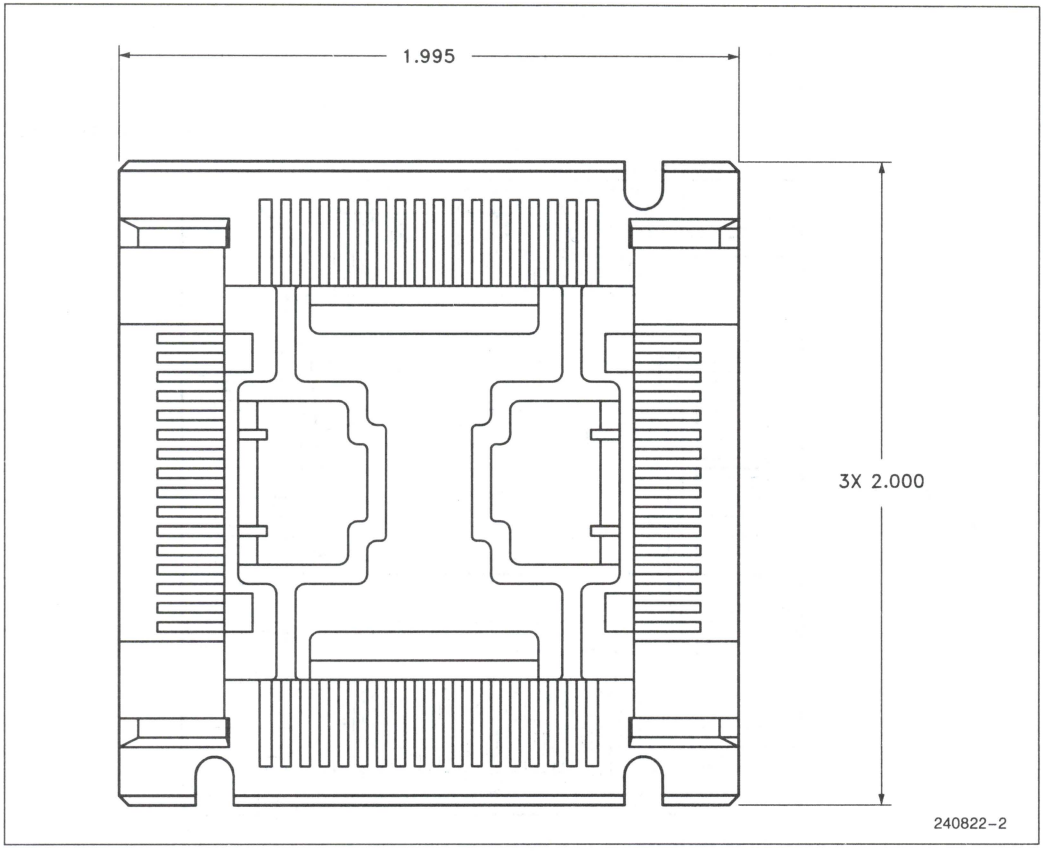


Figure 10-2. 68-Lead Ceramic Flatpack Carrier

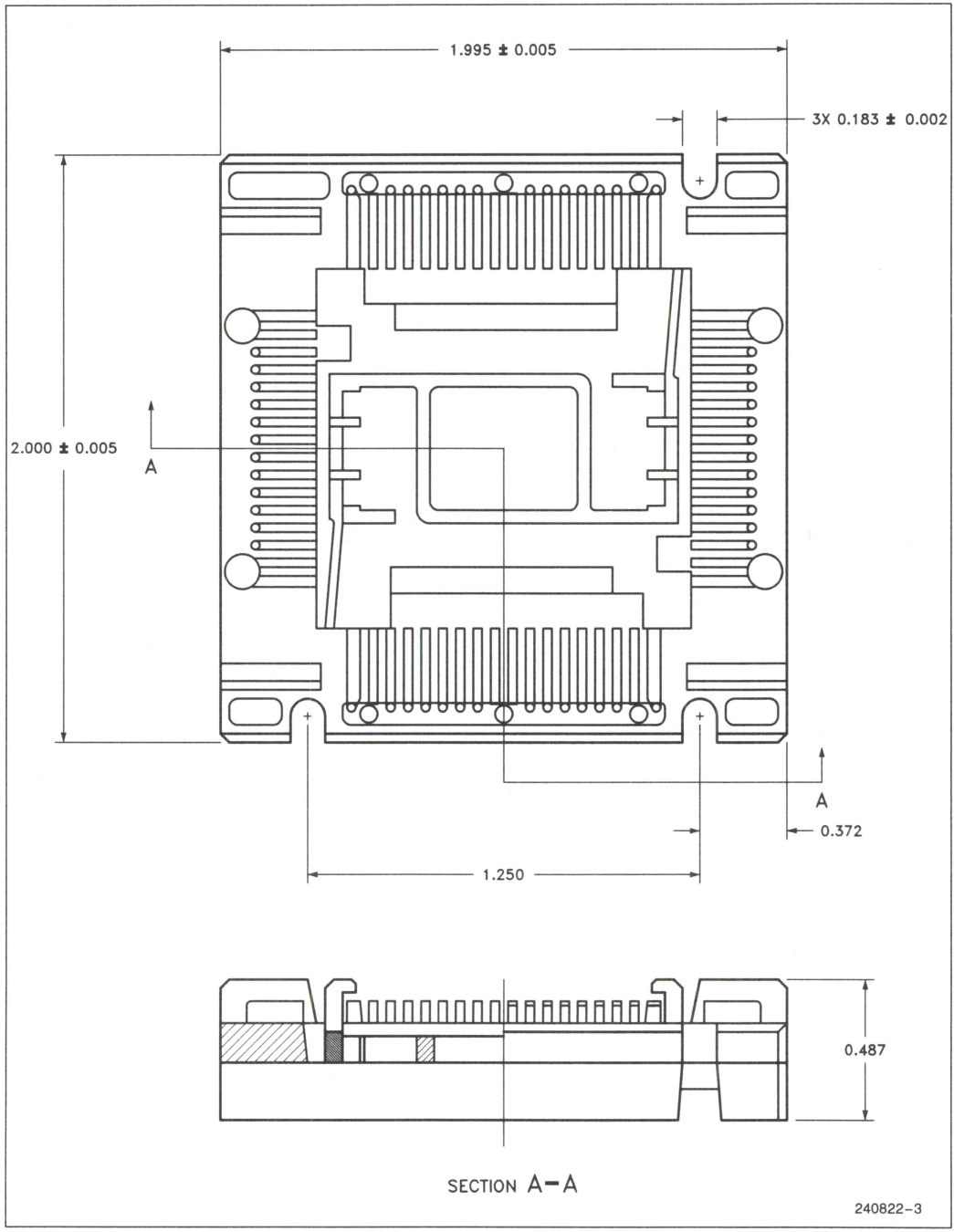


Figure 10-3. 68-Lead Plastic Flatpack Carrier

Trays

Shipping trays are built in compliance with JEDEC thick and thin standard dimensions. Mid-temperature trays can be baked to 140°C while low temperature trays can withstand a maximum sustained temperature of 65°C. Trays are constructed in modified polysulfone (PS) or equivalent for mid-temperature applications and polycarbonate (PC) for low temperature applications because of their high deflection temperature, superior strength, and dimensional stability. All JEDEC trays have the same "X" and "Y" dimensions and are easily stacked for storage and manufacturing.

Intel offers trays for the following:

PQFP: 84 LD, 100 LD, 132 LD, 164 LD, 196 LD thick mid-temperature
84 LD, 100 LD, 132 LD, 196 LD thin mid-temperature
132 LD, 196 LD single unit thick mid-temperature

PGA: 68 LD, 88 LD, 132 LD, 168 LD, 208 LD, 240 LD, 262 LD, 273 LD thick low temperature

PLCC: 28 LD SQ, 28 LD REC, 44 LD SQ, 68 LD SQ, 84 LD SQ thick mid-temperature

TSOP: 32 LD, 40 LD, 56 LD thick and thin mid-temperature

SOP: 32 LD, 44 LD thick mid-temperature

CQFP: 164 LD flat, 196 LD flat thick

MQFP: 44 LD (10 x 10), 64 LD (12 x 12), 80/100 LD (14 x 20) thick and thin mid-temperature

SQFP: 80 LD (12 x 12), 100 LD (14 x 14), 208 LD (28 x 28) thick mid-temperature
80 LD (12 x 12), 100 LD (14 x 14), thin mid-temperature

TQFP: 144 LD (20 x 20), 176 LD (24 x 24) thick and thin mid-temperature

Charts of trays for PQFP, PGA, PLCC, TSOP, PSOP, CQFP, MQFP, SQFP, & TQFP packages are shown on the following pages 10-15 through 10-19. Intel field sales engineers can obtain detailed drawings and specifications upon request.

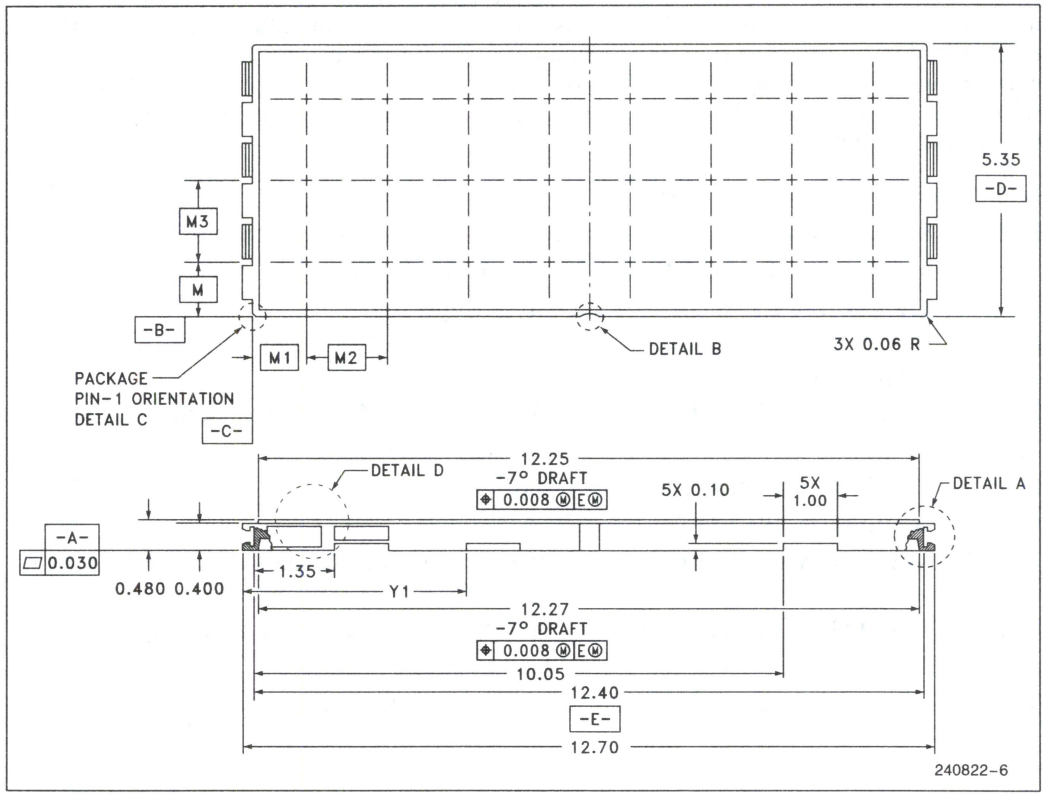


Figure 10-4. Injection Molded Thick JEDEC Tray

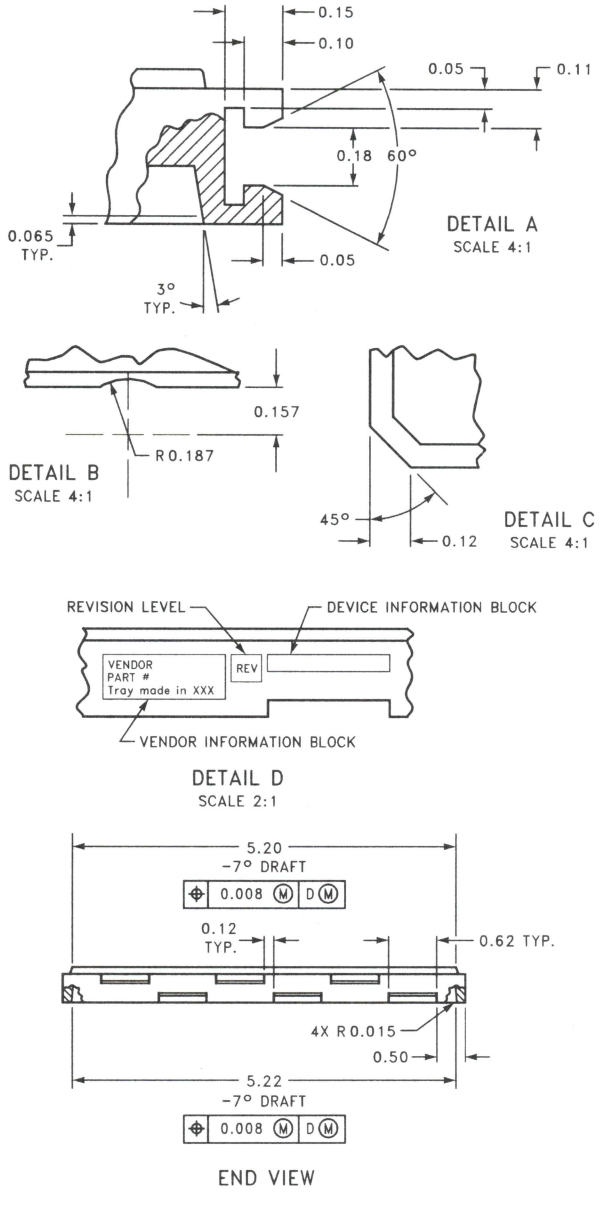


Figure 10-5. Injection Molded Thick JEDEC Tray

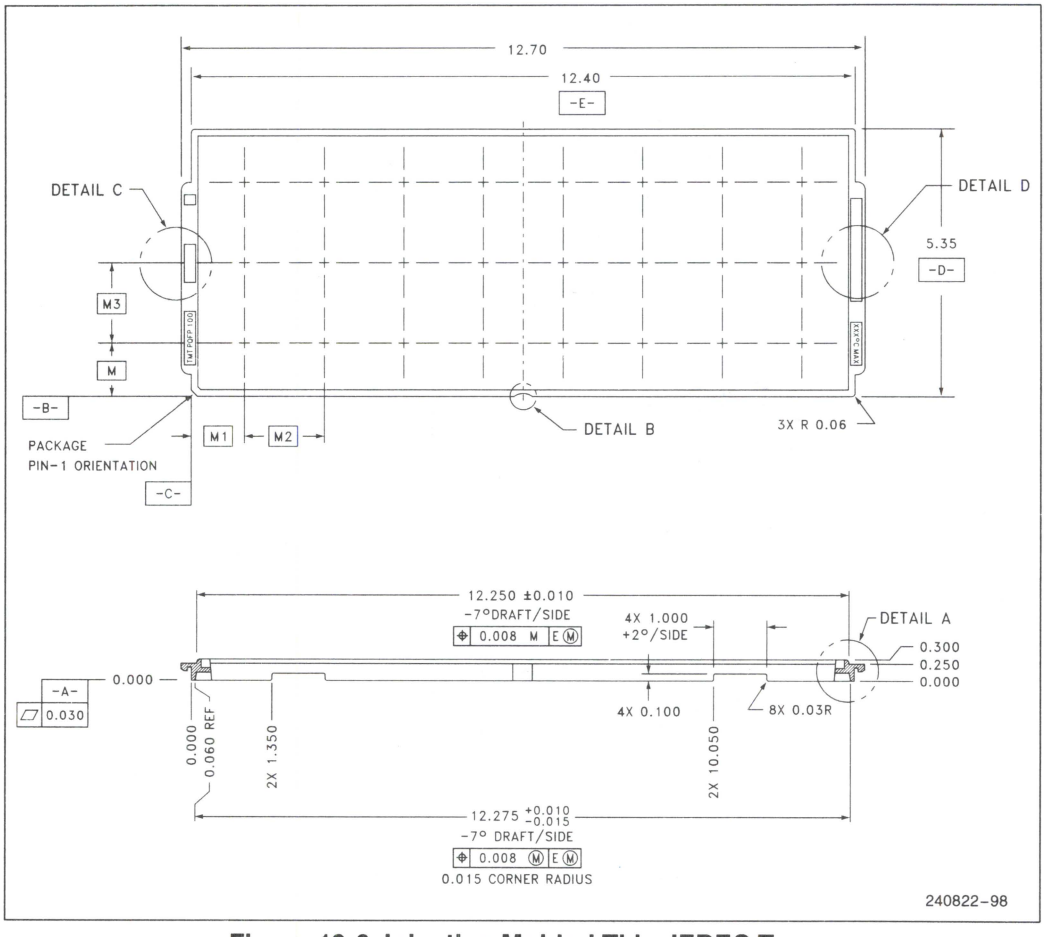


Figure 10-6. Injection Molded Thin JEDEC Tray

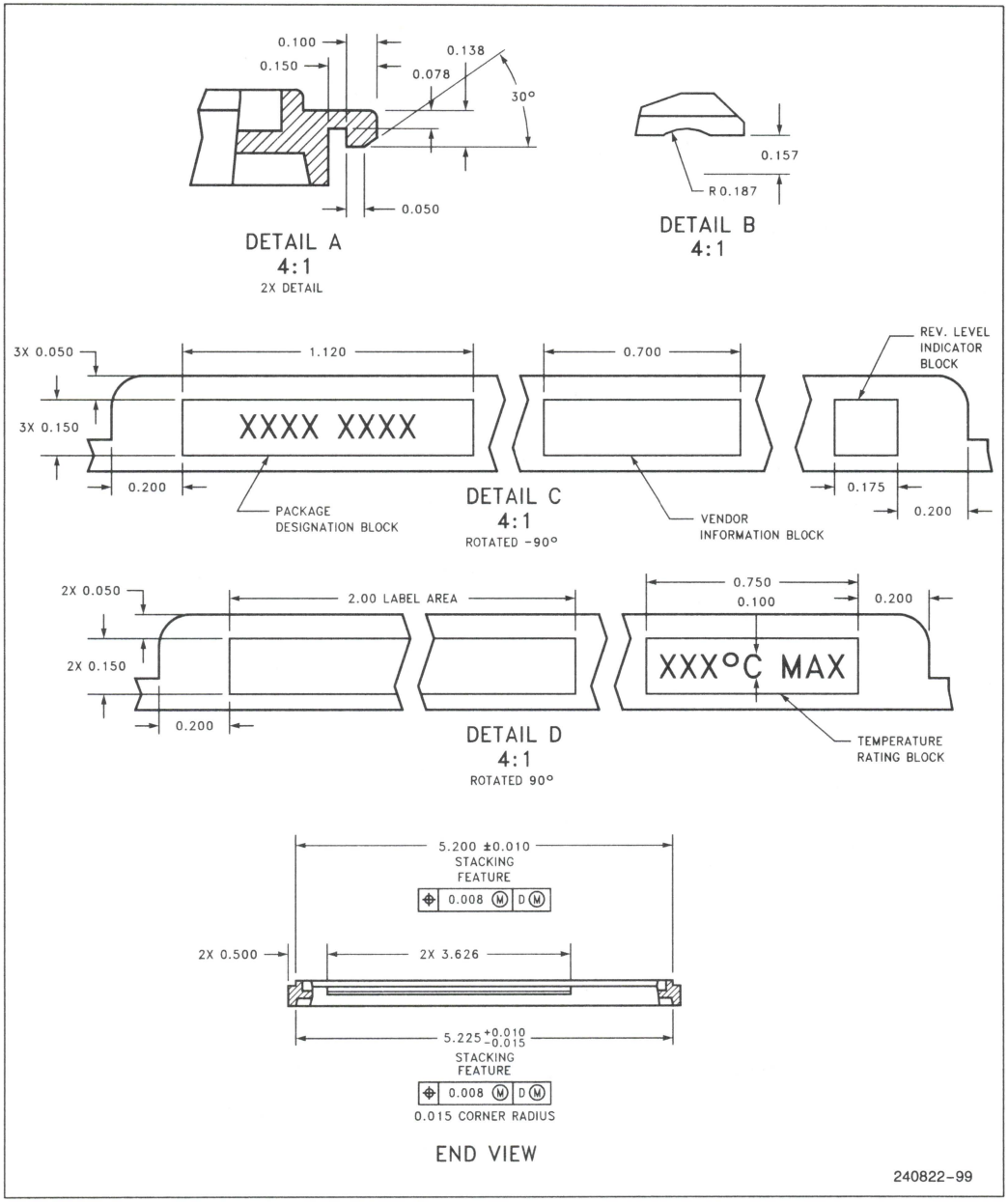


Figure 10-7. Injection Molded Thin JEDEC Tray

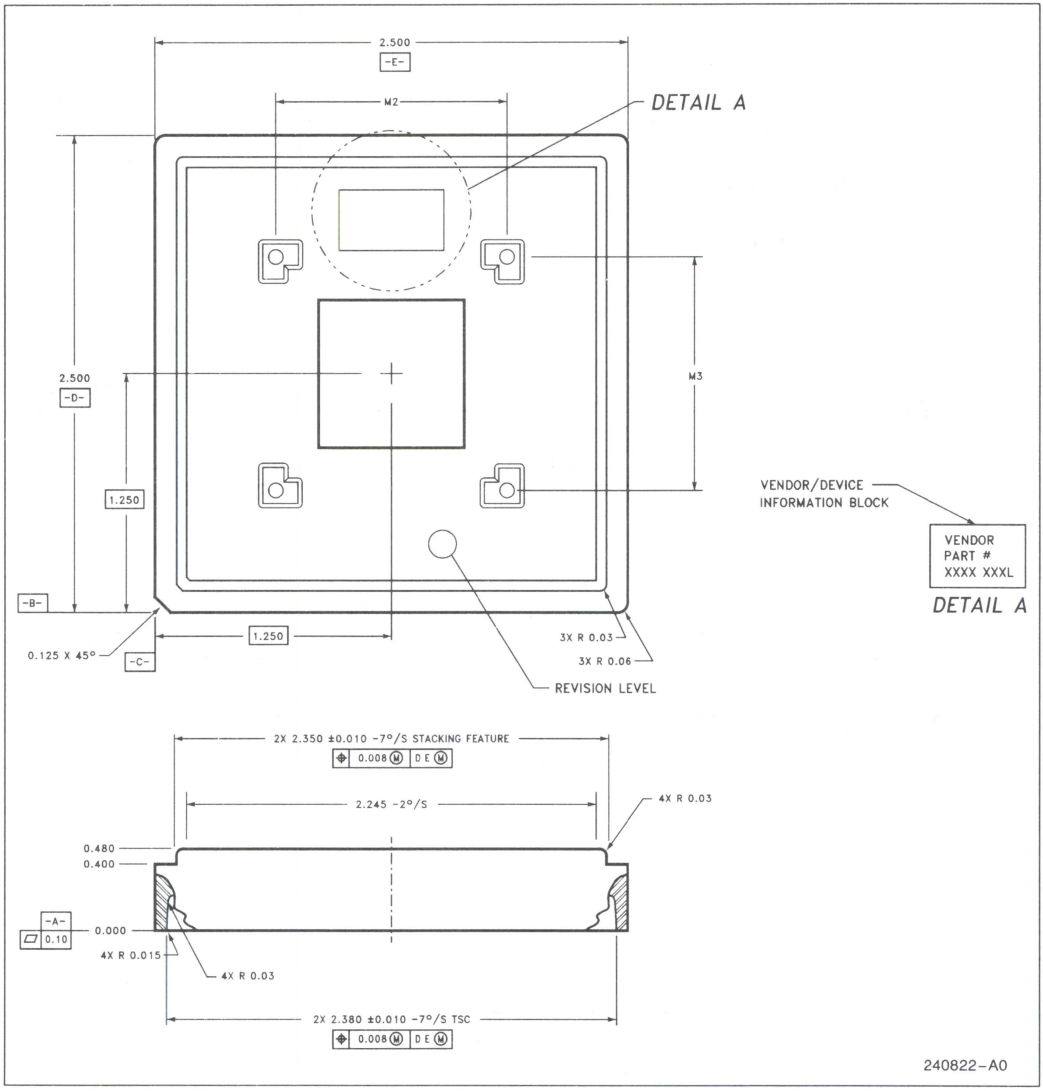


Figure 10-8. Injection Molded Single Unit Tray

Table 10-9. Injection Molded Thick and Thin PQFP JEDEC Tray

PQFP Tray Dimensions						
Pocket Locations	**Symbol**	**84 LD**	**100 LD**	**132 LD**	**164 LD**	**196 LD**
Pocket Cntr Location to Edge Y	M	0.701	0.701	0.824	1.161	1.030
Pocket Cntr Location to Edge X	M1	0.706	0.750	0.944	0.957	1.064
Pocket-Pocket Cntr Distance X	M2	0.999	1.090	1.314	1.498	1.712
Pocket-Pocket Cntr Distance Y	M3	0.987	0.987	1.234	1.514	1.645
# of Rows of Pockets	Rows	5	5	4	3	3
# of Columns of Pockets	Columns	12	11	9	8	7
Total # of Pockets	Pockets	60	55	36	24	21

Table 10-10. Injection Molded Thick PGA JEDEC Tray

PGA Tray Dimensions							
Pocket Locations	**Symbol**	**68 L**	**88 L**	**132 L**	**168 L**	**240 L**	**273 L**
Pocket Cntr Location to Edge Y	M	1.072	1.573	1.556	1.506	1.473	1.456
Pocket Cntr Location to Edge X	M1	1.152	1.077	1.285	1.513	1.446	1.861
Pocket-Pocket Cntr Distance X	M2	1.683	1.708	1.966	2.344	2.377	2.892
Pocket-Pocket Cntr Distance Y	M3	1.603	2.204	2.237	2.337	2.404	2.438
# of Rows of Pockets	Rows	3	2	2	2	2	2
# of Columns of Pockets	Columns	7	7	6	5	5	4
Total # of Pockets	Pockets	21	14	12	10	10	8

NOTE:
All dimensions are in inches.

Table 10-11. Injection Molded Thick PLCC JEDEC Tray

PLCC Tray Dimensions						
Pocket Locations	**Symbol**	**PLCC 28 LD(R)**	**PLCC 28 LD(S)**	**PLCC 44 LD(S)**	**PLCC 68 LD(S)**	**PLCC 84 LD(S)**
Pocket Cntr Location to Edge Y	M	0.670	0.767	0.899	1.079	1.070
Pocket Cntr Location to Edge X	M1	0.755	0.880	0.890	1.163	1.148
Pocket-Pocket Cntr Distance X	M2	0.990	1.064	1.180	1.679	1.684
Pocket-Pocket Cntr Distance Y	M3	0.802	0.954	1.184	1.596	1.605
# of Rows of Pockets	Rows	6	5	4	3	3
# of Columns of Pockets	Columns	12	11	10	7	7
Total # of Pockets	Pockets	72	55	40	21	21

NOTE:
All dimensions are in inches.

Table 10-12. Injection Molded Thick TSOP JEDEC Tray (TSOP Type I)

TSOP Tray Dimensions				
Pocket Locations		**32 LEAD**	**40 LEAD**	**56 LEAD**
Pocket Cntr Location to Edge Y	M	0.477 (12.12)	0.728 (18.49)	0.680 (17.27)
Pocket Cntr Location to Edge X	M1	1.160 (29.46)	1.160 (29.46)	1.160 (29.46)
Pocket-Pocket Cntr Distance X	M2	1.260 (32.00)	1.260 (32.00)	1.260 (32.00)
Pocket-Pocket Cntr Distance Y	M3	0.628 (15.95)	0.649 (16.49)	0.665 (16.89)
# of Rows of Pockets	Rows	8	7	7
# of Columns of Pockets	Columns	9	9	9
Total # of Pockets	Pockets	72	63	63

Table 10-13. Injection Molded Thin TSOP JEDEC Tray (TSOP Type I)

TSOP Thin Tray Dimensions				
Pocket Locations		**32 LEAD**	**40 LEAD**	**56 LEAD**
Pocket Cntr Location Y	M	0.348	0.567	0.500
Pocket Cntr Location X	M1	0.571	0.679	0.679
Pocket-Pocket X	M2	1.024	1.004	1.004
Pocket-Pocket Y	M3	0.388	0.468	0.618
# of Rows of Pockets	Rows	13	10	8
# of Columns of Pockets	Columns	12	12	12
Total # of Pockets	Pockets	156	120	96

Table 10-14. Injection Molded Thick PSOP JEDEC Tray (TSOP Type II)

PSOP Tray Dimensions			
Pocket Locations		**32 LEAD**	**44 LEAD**
Pocket Cntr Location to Edge Y	M	0.821 (20.85)	0.821 (20.85)
Pocket Cntr Location to Edge X	M1	1.280 (32.51)	1.251 (31.78)
Pocket-Pocket Cntr Distance X	M2	1.230 (31.24)	1.414 (35.92)
Pocket-Pocket Cntr Distance Y	M3	0.927 (23.55)	0.927 (23.55)
# of Rows of Pockets	Rows	5	5
# of Columns of Pockets	Columns	9	8
Total # of Pockets	Pockets	45	40

NOTE:
Dimensions are in inches (millimeters).

Table 10-15. Injection Molded Thick Flat CQFP JEDEC Tray

CQFP Flat Leads Tray Dimensions			
Pocket Locations		**164 LD Flat**	**132/196 LD Flat**
Pocket Cntr Location to Edge Y	M	2.675	2.675
Pocket Cntr Location to Edge X	M1	1.700	1.700
Pocket-Pocket Cntr Distance X	M2	3.000	3.000
Pocket-Pocket Cntr Distance Y	M3	—	—
# of Rows of Pockets	Rows	1	1
# of Columns of Pockets	Columns	4	4
Total # of Pockets	Pockets	4	4

NOTE:
All dimensions are in inches.

Table 10-16. Injection Molded Thick and Thin MQFP JEDEC Tray

MQFP Thick and Thin Tray Dimensions					
Pocket Locations		**44 LD (10 x 10)**	**64 LD (12 x 12)**	**80/100 (14 x 20) Thick**	**80/100 (14 x 20) Thin**
Pocket Cntr Location Y	M	0.720	0.608	0.843	0.608
Pocket Cntr Location X	M1	0.680	0.701	1.034	0.886
Pocket-Pocket X	M2	0.736	0.846	1.148	1.063
Pocket-Pocket Y	M3	0.782	0.827	0.916	0.827
# of Rows of Pockets	Rows	6	6	5	6
# of Columns of Pockets	Columns	16	14	10	11
Total # of Pockets	Pockets	96	84	50	66

Table 10-17. Injection Molded Thick and Thin SQFP JEDEC Tray

SQFP Thick and Thin Tray Dimensions				
Pocket Locations		**80 LD (12 x 12)**	**100 LD (14 x 14)**	**208 LD (28 x 28)**
Pocket Cntr Location Y	M	0.608	0.608	1.218
Pocket Cntr Location X	M1	0.701	0.701	1.100
Pocket-Pocket X	M2	0.846	0.846	1.457
Pocket-Pocket Y	M3	0.827	0.827	1.457
# of Rows of Pockets	Rows	6	6	3
# of Columns of Pockets	Columns	14	14	8
Total # of Pockets	Pockets	84	84	24

Table 10-18. Injection Molded Thin and Thick TQFP JEDEC Tray

TQFP Thick and Thin Tray Dimensions			
Pocket Locations		**144 LD (20 x 20)**	**176 LD (24 x 24)**
Pocket Cntr Location Y	M	0.691	0.815
Pocket Cntr Location X	M1	0.701	0.815
Pocket-Pocket X	M2	1.000	1.197
Pocket-Pocket Y	M3	0.992	1.240
# of Rows of Pockets	Rows	5	4
# of Columns of Pockets	Columns	12	10
Total # of Pockets	Pockets	60	40

OVERVIEW

Intel's JEDEC Tray Reclamation Program pays cash for 3M JEDEC trays returned in reusable condition. Not only does the program offer you a cash reimbursement 25 percent higher than the industry standard, but it lowers the cost of plastic shipping trays, employs the handicapped and reduces environmental waste.

To faciliate this program, Intel has established a relationship with Gompers Rehabilitation Center for the handicapped. Gompers is a non-profit organization located in Phoenix that receives, inspects, sorts, and cleans all used trays. Intel currently supplies 78 percent of the production and job training for the disabled workers at Gompers. Nearly 70 disabled workers are employed in box assembly and tray recycling for Intel.

HOW THE PROGRAM WORKS:

1. *Trays Ship to Gompers*

   To minimize tray damage and maximize your refund, tightly package your trays. Intel pays all shipping costs. When shipping trays to Gompers, ship to the address listed below, but bill your shipping costs to Intel.

Ship Trays to This Address:	Bill Shipping Costs to This Address:
Gompers Rehabilitation Center 6601 N. 27th Ave Phoenix, Arizona 85017	Intel Corporation 5000 W. Chandler Blvd. Chandler, Arizona 85226

2. *Gompers Inspects, Sorts and Cleans Used Trays*

   Good trays are returned to Intel for reuse. All damaged 3M trays are recycled back to the 3M factory grinder for reuse in new trays. All non-3M trays are sent to a plastics reclamation vendor to be used in a variety of applications. No trays go to landfills.

3. *You Receive a Reimbursement Check Within 30 Days*

   There is one reimbursement rate assigned to reusable high temp (black) trays and another for reuseable low temp (blue) shipper trays. Cash reimbursements are only paid for good trays. You will be paid by check within 30 days of receipt of trays.

   Intel initiated the JEDEC Tray Reclamation Program in 1989 and revamped it in 1992 to include cash reimbursement. Intel forecasts that by 1994 at least 34 percent of the 3M JEDEC trays used to ship product will be returned for recycling.

For more information, please contact your Field Sales Engineer or Regional Customer Service Manager.

Table 10-19. Carrier Tape Dimensions by Package

Millimeters	Carrier Tape Sizes					
	16 mm	**24 mm**	**32 mm**	**44 mm**	**44 mm**	**44 mm**
Use for These Packages	PLCC 20 LD	PLCC 28 LD (REC) 28 LD (SQ) 32 LD (REC)	PLCC 44 LD 52 LD PQFP 84 LD TSOP 40 LD 32 LD 56 LD	PLCC 68 LD PQFP 100 LD 132 LD	PLCC 84 LD	PSOP 44 LD
E1	1.65–1.85	1.65–1.85	1.65–1.85	1.65–1.85	1.65–1.85	1.65–1.85
Single/ Double Sprocket	Single	Single	Double	Double	Double	Double
P_0	3.9–4.1	3.9–4.1	3.9–4.1	3.9–4.1	3.9–4.1	3.9–4.1
P_1*	—	—	—	—	—	—
R	30.0 Min	30.0 Min	50.0 Min	50.0 Min	50.0 Min	100.0 Min
T	0.25–0.35	0.25–0.35	0.25–0.35	0.25–0.35	0.25–0.35	0.25–0.35
W	15.7–16.3	23.7–24.3	31.7–32.3	43.7–44.3	43.7–44.3	55.7–56.3
Qty Units Per Reel (Max)	1000	750	500	350	250	450

NOTE:
All dimensions are in millimeters.
*P_1—This dimensions can be any multiple of 4 mm.

SHIPPING FORMATS

Desiccant Pack Materials

All PSMCs are shipped in desiccant pack. For a thorough discussion of the packing process (bake and bag) and handling considerations unique to PSMCs, please consult Chapter 7, which addresses moisture sensitivity of PSMC's.

Intel uses the following materials in desiccant pack:

- **Moisture Barrier Bag (MBB).** Inside the shipping box is a moisture barrier bag containing components. The opaque MBB is constructed of three layers: a conductive polyethylene inner layer for sealing, an aluminum film mid-layer, and a tyvek outer layer. The bag meets MIL-STD-81705 TYPE I for electrostatic discharge (ESD) and mechanical stability. The measured water vapor transmission rate (WVTR) of the bag is better than the MIL-STD requirements for moisture protection.

  A "warning" label on the bag outlines precautions that should be taken with desiccant-packed units. A desiccant barcode label is also affixed to the bag.

- **Desiccant.** Each MBB contains one or more pouches of desiccant to absorb moisture that may be present in the bag. The desiccant is supplied in one-unit pouches. The number of pouches required is a function of the bag surface area.

- **Humidity Indicator Card (HIC).** Along with the desiccant pouches, each MBB contains a humidity indicator card. This card is a military-standard moisture indicator and is included to show the user the approximate relative humidity (RH) level within the bag. The HIC is reversible and can be reused.

- **Labels.** The desiccant barcode label (shown in Figure 10-11), mentioned above in the section on MBBs, contains the date that the bag was sealed (MM/DD/YY). The remaining storage life of the units in the bag is determined from this date.

  The "warning" label attached to the outside of the MBB outlines precautions that must be taken when handling desiccant-packed units if they are to be kept dry.

- **Shipping Box.** The barcode label on the shipping box will indicate that desiccant-packed material is included. This label will indicate the seal date of the enclosed MBB, and thus, the remaining shelf life.

Shipping Boxes and Cartons

Intel products are placed in tubes or trays, or on reels, then packed for shipment in a box made of corrugated fiberboard with an inner coating of conductive carbon that prevents electrostatic damage. Various materials, such as bubble wrap or antistatic foam end pads, are used for cushioning inside the box. Outer boxes are used for increased protection during shipping. All packing materials are either conductive, static dissipative, or antistatic, and meet the electrostatic discharge (ESD) requirements of EIA standard 541.

Labeling Information

- **Tube and Reel Labels.** Tube labels with information on lot traceability, part and spec numbers, quantity of parts, and ROM and PROM codes are available by special order. Reel labels are standard and provide the same information. Customer part number references can be included on either type of label, also by special order.
- **Box Labels.** Bar-coded labels for each box are standard on Intel product shipments. Box labels provide all the information on the tube labels, show order packing and shipping information, and allow more space to define special requirements. Figure 10-11 shows detail of a standard box barcode label.

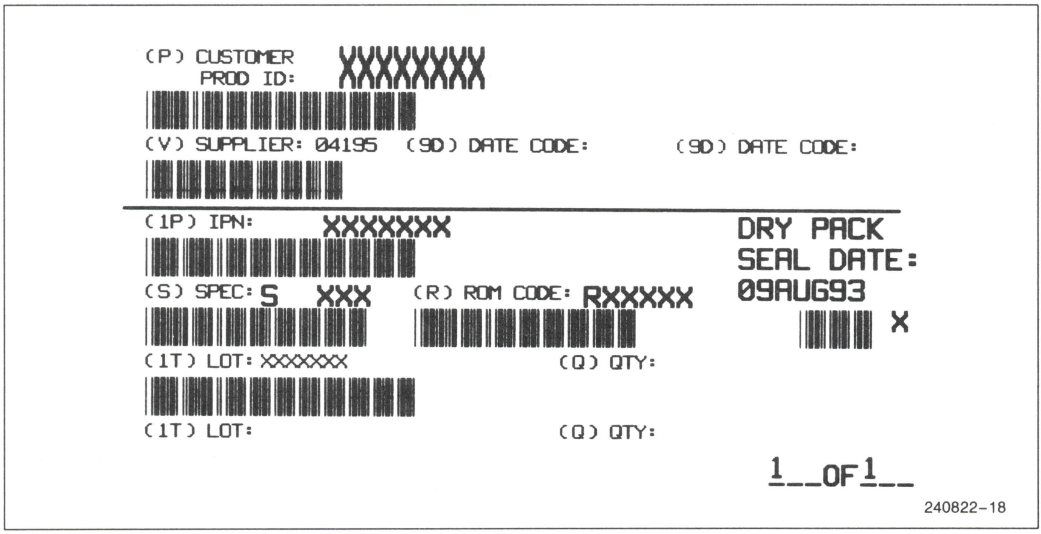


Figure 10-11. Desiccant Barcode Label

REVISION SUMMARY

The main differences between the 240822-004 revision and the -003 version are the following:

- Added Thin SQFP trays
- Updated tray Recycle Program

International Packaging Specifications

11

CHAPTER 11
INTERNATIONAL PACKAGING SPECIFICATIONS

ELECTRONIC INDUSTRIES ASSOCIATION OF JAPAN (EIAJ)

EIAJ publishes the following general rules and standards as they apply to preparation of outline drawings on integrated circuits:

Number	Nomenclature
SD-74-1	General rules for the preparation of outline drawings of semiconductor devices
SD-74-2	Outline drawings of semiconductor devices
SD-74-2 add 1	Outline drawings of semiconductor devices -1
SD-74-2 add 2	Outline drawings of semiconductor devices -2
IC-74-1	Outline drawings of integrated circuits
ED-7402	Small outline packages (SOPs)
IC-74-2	Thin small outline packages (TSOPs)
ED-7403-1	Dual in-line packages (DIPs)
IC-74-4	Quad flat packages (QFPs)
ED-7404-1	Quad flat packages (QFPs, fine pitch)
IC-74-5	Zig-zag in-line packages (ZIPs)
ED-7406	Small outline J-lead packages (SOJs)
ED-7407	Quad flat J-lead packages (QFPs)
ED-7408	Pin grid array packages (PGAs)
ED-7413	Small in-line packages (SIPs)

JOINT ELECTRON DEVICE ENGINEERING COUNCIL (JEDEC)

JEDEC Publication 95 lists all package outlines.

MIL STANDARDS

The following military standards include specifications required to meet U.S. Military requirements:

- MIL-M-38510 General Specifications for Microcircuits
- MIL-STD-883 Test Methods/Procedures for Microelectronics

SEMICONDUCTOR EQUIPMENT AND MATERIALS INSTITUTE, INC. (SEMI) STANDARDS

For a list of SEMI standards, reference the *Book of SEMI Standards,* 1990, Vol. 4, Packaging Division, 605 E. Middlefield Road, Mountain View, CA 94043, U.S.A. Phone: (415) 964-5111. FAX: (415) 967-5375. TELEX: 856-777 SEMI-MNTV.

INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC) STANDARDS

Number	Nomenclature
ANSI/IPC-S-815B	General requirements for soldering electronic connections
ANSI/IPC-SM-780	Component packaging and inter-connecting, with emphasis on surface mounting
ANSI/IPC-SM-782	Surface mount land patterns
ANSI/IPC-SM-786	Impact of moisture on plastic I/C package cracking

For a list of additional IPC standards, contact: IPC, 7380 N. Lincoln Ave., Lincolnwood, Illinois, 60646. Phone: (708) 677-2850.

Glossary

12

CHAPTER 12
GLOSSARY

A

Access hole: A hole or series of holes in successive layers of a multilayer board that provide(s) access to the surface of the land in one or more layers of the board.

All-metal package: A hybrid circuit package made solely of metal, excluding glass or ceramic.

Alternating current resistance: The resistance offered by any circuit to the flow of alternating current.

Alumina: Aluminum oxide. Alumina substrates are made of formulations that are primarily alumina.

Ambient: The environment that surrounds a system or component.

Ampere: The unit used for measuring the quantity of an electric current flow. One ampere represents a flow of one coulomb per second.

Annular ring: The portion of a conductive material that completely surrounds a hole.

Anode: The electrode from which the forward current flows within a device.

Application-specific integrated circuit (ASIC): An integrated circuit chip customized for a specific product.

Area array tape-automated bonding: Tape-automated bonding in which edge-located pads and additional pads on the inner surface area of a chip are addressed in the bonding scheme.

ATE: Automated Test Equipment.

A/T QRE: Assembly/Test Quality & Reliability Engineering.

Auger: A surface analysis technique for detecting the chemical composition of material.

B

Base plane: The plane through the lowest point of the mounting surface of the package, except for packages using stand-offs.

Bipolar: A device in which both majority and minority carriers are present. Bipolar and metal-oxide semiconductor (MOS) are the two most common device types.

Body: The main or largest portion of a connector, to which other portions are attached or connected.

Bonding: The joining of two materials; for example, the attachment of wires to an integrated circuit or the mounting of an integrated circuit to a substrate.

Bonding pads: Areas of metallization on the integrated circuit die that permit connection of fine wires or circuit elements to the die.

Bond schedule: Bonding machine set-up parameters.

Bond window: The acceptable range of each bonding variable, including time, force, power, and temperature.

Bump: A means of providing a connection to the terminal area of a device. A small mound is formed on the device or substrate pads and is used as a contact for facedown bonding.

Bump contacts: Contacting pads that rise substantially above the surface level of the chip.

Bumped tape: A tape used in the tape-automated bonding process whose innerlead bond sites have been formed into raised metal bumps, thus eliminating the need for bumps on the chip itself.

Buried via: A via hole not extending to the surface.

Burn-in: The process of screening out marginal component parts by exposing them to elevated temperatures and voltage stress.

Butt lead: A lead count of surface mount devices in which pin tips contact the PC board.

C

Ceramic: Inorganic, nonmetallic, clay, or glasslike material whose final characteristics are produced by subjection to high temperatures.

Ceramic quad flatpack (CQFP): An aluminum ceramic integrated circuit package with four sets of leads extending from the sides and parallel to the base.

CERDIP: A dual in-line package composed of a ceramic header and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerpack: A flatpack composed of a ceramic base and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerquad: A ceramic equivalent of plastic leaded chip carriers, consisting of a glass-sealed ceramic package with J-leads and ultraviolet window capability.

Chip: The individual circuit or component of a silicon wafer, also known as a die.

Chip carrier: An integrated circuit package, usually square, with a chip cavity in the center. Its connections are normally on all four sides.

Circuit: The interconnection of a number of components in one or more closed paths to perform a desired electrical or electronic function.

C-mode scanning acoustic microscope (CSAM): An analytical tool for the nondestructive evaluation of microelectronic packages via acoustic waves.

Coefficient of linear thermal expansion (CTE): The change in linear dimension per degree change in temperature, usually expressed as parts per million per degree Celsius.

Complementary metal-oxide semiconductor (CMOS): Logic in which cascaded field-effect transistors of opposite polarity are used to minimize power consumption.

Component: An individual functional element in a physically independent body that cannot be further reduced or divided without destroying its stated function. Examples include resistors, capacitors, diodes, and transistors.

Component lead: The solid or stranded wire or formed conductor that extends from a component and serves as a mechanical or electrical connection, or both.

Component lead hole: A hole used for the attachment and electrical connection of a component termination, including pins and wires, to a PC board.

Conductance: A measure of the ability of a material to conduct an electrical current.

Conductivity, electrical: The capability of a material to carry an electrical current.

Conformal coating: An insulative coating that conforms to the configuration of the object being coated.

Connector: Generally, all devices used to provide rapid connect/disconnect service for electrical cable and wire terminations, board to board.

Convection: A conveying or transference of heat or electricity by moving particles of matter.

D

Dambar: A portion of the lead frame that prevents mold compound from flowing to the ends of the lead frame.

Design of experiments: A systematic methodology for planning an experiment in order to consider all input and output variables.

Dicing: The separation of a semiconductor wafer into individual dies.

Die: The individual semiconductor element or integrated circuit, also known as a chip.

Die bonding: The attachment of an integrated circuit chip to a substrate or header.

Die paddle: The central portion of the lead frame, onto which the die and adhesive are placed during die attach.

Discrete: A term applied to single-element electrical components.

Dual in-line package (DIP): A component that terminates in two straight, parallel rows of pins or lead wires.

E

EIA: Electronic Industries Association.

EIAJ: Electronic Industries Association of Japan.

Electrode: A conductor through which a current enters or leaves an electrolytic cell.

Electronic packaging: The technical discipline of designing a protective enclosure for an electronic circuit so that it will both survive and perform effectively under a variety of environmental conditions.

Electrostatic discharge (ESD): The instantaneous transfer of charges accumulated on a non-conductor to a conductor, into ground.

Encapsulate: To seal or cover an element or circuit for mechanical and environmental protection.

Energy-dispersive X-ray (EDX) analysis: Normally, using electron beam excitation in the scanning electron beam microscope.

Eutectic: The minimum melting point of a combination of two or more metals.

External leads: Electronic package conductors for input and output signals, power, and ground.

F

Facedown bonding: A method of attaching a component or circuit chip to a substrate by inverting the chip and bonding chip contacts to the mirror-image contact points on the substrate.

Failure mode: Failure at the macro level, i.e., the observed effect of failure.

Farad: A unit of electric capacity.

Flatpack: An integrated circuit package whose leads extend from the sides and are parallel to the base.

Flip-chip: A chip that has bumped termination spaced on the face of the device and is designed for facedown mounting.

Footprint: The area occupied on a substrate by a component or element.

Frequency: Of an electric current, the number of hertz, or completed alternations per second.

Frit: A relatively low softening point of glass composition.

G

Gate array: A semicustom product, implemented from a fully diffused or ion-implanted semiconductor wafer carrying a matrix of identical primary cells arranged into columns with routing channels between them in x and y directions.

Ground: A common reference point for circuit returns, shielding, or heat sinking.

H

Hermetic: Sealed so that an object is gas-tight, to a specific rate, normally less than 1×10^{-6} cc/sec of helium.

High-density plastic quad flatpack (HD-PQFP): A package with greater than 196 leads and a pitch of 0.4 mm.

Hot dip: The process of covering a surface by dipping it into a molten bath of coating material.

I

I-lead: A surface mount device lead whose ends contact the board at a 90° angle; also called a butt joint.

Imidization: The reaction comprises acylation of the diamine with dianhydride in a polar solvent to give poly(amic acid), conversion of polyamic acid to polyimide with subsequent loss of small molecules, such as water.

Inductance: The resistance of an electric circuit to any change of current during the building up or decaying of a self-induced magnetic field. This property introduces a delay in current change, with resulting operational delay.

Infrared (IR): Radiant energy that is characterized by wavelengths longer than visible red (0.78 to 100 μm or 0.030 to 3.9 mils).

Input/output (I/O) terminal: A chip or package connector that interconnects the chip to the package, or one package level to the physically adjacent level in the hierarchy.

Insert: To assemble components, manually or automatically, into a PC board.

Insert cavity: A defined hole in the connector insert into which the contacts are inserted.

Insertion mount: The electrical and mechanical connection of a component to the surface of a conductive pattern utilizing component holes.

Insulators: A class of materials with high resistivity; materials that do not conduct electricity.

Integrated circuit (IC): A microcircuit consisting of multiple interconnected elements inseparably associated and formed on or within a single substrate to perform an electronic circuit function.

Integrated circuit chip: The active semiconductor element that is the functional part of the integrated circuit.

Intermetallic compound (IMC): An intermediate phase—homogeneous phase whose composition range does not include any pure metal—in an alloy system that has a narrow range of composition, but has an atomic bonding that can be of several types.

J

JEDEC: Joint Electronic Device Engineering Council.

J-lead: A surface mount device whose leads are formed into a "J" pattern, folding under the device body.

K

Kirkendall voiding: The formation of voids as a result of a disproportional diffusion rate between two neighboring materials.

Kovar: An alloy of 53% iron, 17% cobalt, 29% nickel, and trace elements, with a thermal expansion matching alumina ceramics and sealing glasses.

L

Laminate: A product made by bonding two or more layers together, usually of different materials, under heat and pressure to form a single structure.

Land Pattern: Also called footprint or Pad, define the site where components are to be soldered to a PC board.

Large-scale integration (LSI): Usually, monolithic digital integrated circuits with a complexity of 100 or more gates or gate-equivalent circuits.

Laser bonding: Effecting a metal-to-metal bond of two conductors by welding the two materials together with a laser beam as a heat source.

Lead: A conductive path, usually self-supporting; the portion of an electrical component that connects it to the outside world.

Lead (Pb): A soft, heavy metal used in solder compositions and other alloys.

Leaded chip carrier: A plastic or ceramic chip carrier with compliant leads for termination.

Leaded surface mounting: The surface mounting of components to a substrate by means of component leads and solder joints.

Lead frame: The metallic portion of the device package that completes the electrical connection path from the die or dies and from ancillary hybrid circuit elements to the outside world.

Leadless chip carrier (LCC): An integrated circuit package that allows surface mounting of components directly into the substrate by means of solder joints.

Lead wires: Wire conductors used for intraconnections requiring fine wires or for interconnections that include input/output.

M

Marking: A method of identifying packages with part numbers, manufacturer code, and other information.

Mobile dislocations: Atomic line defects in polycrystalline material.

Modulus of elasticity: The ratio of stress to strain in an elastic material.

Moisture barrier bag (MBB): A strong, three-ply bag that is electrostatic discharge (ESD)-safe and allows minimal moisture transmission. The bag is intended to protect enclosed devices from moisture exposure and should not be opened till the devices are ready for board mounting.

Mounting hole: A hole used for the mechanical mounting of a PC board or for the mechanical attachment of components to the board.

Multilayer molded package (MM): A PQFP with enhanced performance achieved by a pair of power and ground planes. These planes significantly reduce the power-ground capacitance, making the package ideal for high-speed device operation.

O

Ohm: A unit of electrical resistance.

P

Package: An enclosure for a single element, integrated circuit, or hybrid circuit. It provides hermetic or nonhermetic protection, determines the form factor, and serves as the first-level interconnection externally for the device by means of package terminals.

Pad: The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections.

Piezoresistive elements: Pressure-sensitive resistors.

Pin grid array (PGA): A square package with pins covering the entire bottom surface at a pitch of 0.1 in. or 0.05 in., perpendicular to the plane of the package.

Pitch: The nominal distance from center to center of adjacent conductors.

Plastic leaded chip carrier (PLCC): A package with J-leads on all sides.

Plating: Metallic deposit on a surface, formed either chemically or electrochemically.

PPE: Plastic Package Engineering.

PQFP: Plastic quad flatpack.

Printed circuit board: A board with printed-on components as well as point-to-point connections.

PSMC: Plastic surface mount component.

Q

Quad flatpacks (QFPs): A generic term for surface mount technology flat packages with leads on all four sides; commonly used to describe chip carrier-like devices with gull-wing formed leads. The lead pitch for QFPs is in metric. The packages have no corner bumpers.

R

Real estate: The surface area of an integrated circuit or substrate.

Reflow: A soldering process that uses solder paste preprinted in a pattern on the PC board and heats the devices in place to make connections.

Resistance: The property of an electric circuit that determines, for a given current, the rate at which electric current is converted into heat. The power converted can be calculated by multiplying the current squared by the resistance.

Resistivity: The ability of a material to resist the passage of electric current.

Resistor: A device that offers resistance to the flow of electric current in accordance with Ohm's law: R = E/I, where R = resistance, E = voltage, and I = current.

RH: Relative Humidity.

S

Scanning electron microscope (SEM): A microscope that makes use of a scanning beam of electrons to image detail less than 100 angstroms in size (surface only).

Shrink DIP: A package resembling a DIP, with a lead pitch of 0.07 in., used in applications requiring high mounting densities.

Single in-line memory module (SIMM): A module to which external connection is made by a row of conductors along one side.

Single in-line package (SIP): A package with leads on a single side only.

Small outline with J-leads (SOJ): A small outline package with J-leads.

Small outline package (SOP): A package with two rows of narrowly spaced gull-wing leads.

Solderability: The property of a component lead to be wetted by molten solder under specified conditions.

Soldercoat: A process used to apply solder to package leads directly from a molten solder bath.

Specific gravity: The ratio of the weight of a given volume of a substance to the weight of an equal volume of water; also known as relative density.

Surface mount technology (SMT): Electrical and mechanical connection of components to the surface of a conductive pattern without using component holes. Components mounted in this manner are known as **surface mount devices (SMDs)** or **surface mount components (SMCs)**.

T

Tape-automated bonding (TAB): A chip interconnect process that can be used as an alternative to wire bonding.

Tensile strength: The greatest longitudinal tensile-strength stress a substance can bear without tearing apart or rupturing.

Terminal: A metallic termination device used for making electrical connections.

Thermal expansion: The expansion of a material when subjected to a temperature change.

Thermosonic bonding: The bonding of wires to metal pads on an integrated circuit by means of heat and ultrasonic scrubbing of wire into the pad to create a metallurgical bond.

Through-hole mounting: The electrical connection of components to the surface of a conductive pattern using component holes.

Tin whisker: A hairlike, single crystal growth formed on the metal surface.

Thin small outline package (TSOP): A plastic, surface mount memory package that features 0.5 mm pitch gull-wing leads located on two sides of the package.

Transmission electron microscope (TEM): A microscope used to obtain high-resolution images with a transmitted electron beam by electron lens imaging rather than scanning.

U

Ultrasonic bond: A bond formed when a wire is pressed against a bonding pad and the pressing mechanism is ultrasonically vibrated at a high frequency above 10 kHz.

V

Vapor phase soldering (reflow): The technique for soldering reflow to form package interconnections. The energy produced by the condensation of an inert vapor is used to heat solder joints.

Visual index: A visible mark, chamber, notch, tab, or depression indicating the position of pin 1, used to determine the orientation of an integrated circuit.

W

Wave soldering: A process in which PC boards are brought in contact with the surface of continuously flowing and circulating solder.

WDX: Wave-length dispersive X-ray analysis.

Wire bond: A completed wire connection that includes all its constituents and provides electrical continuity between the semiconductor die and a terminal.

Appendix A

13

APPENDIX A
NON-JEDEC TRAYS

EIAJ-STYLE TRAYS

Some of Intel's QFP packages are shipped in non-JEDEC trays. In fact, many EIAJ-style tray designs existed before JEDEC had approved corresponding QFP tray designs. The following pages contain dimensional information on the EIAJ-style trays which Intel supports today. All EIAJ-style trays are constructed of ESD-resistant plastic. The following Low-Temperature Trays can withstand a maximum ambient temperature of 50 degrees Celsius, while the Mid-Temperature Trays can withstand 125 degrees Celsius.

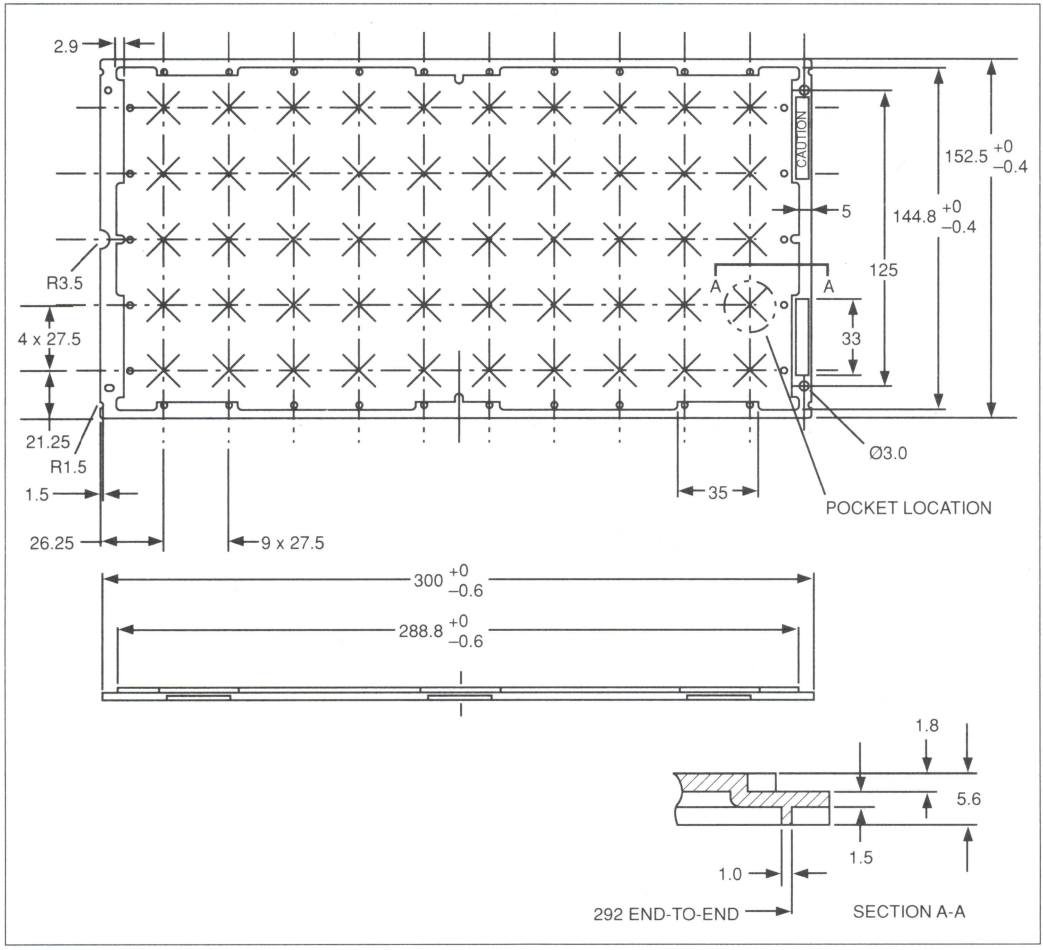


Figure A-1. EIAJ-Style 44 Lead QFP Mid-Temperature Tray

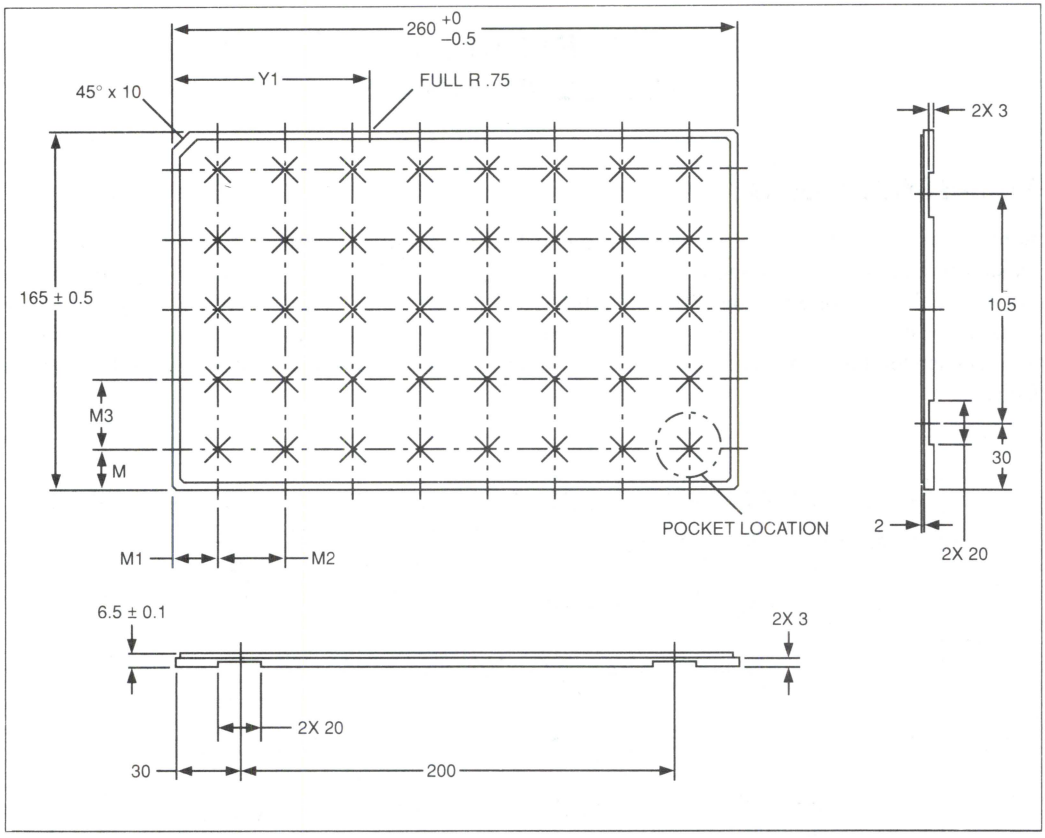


Figure A-2. EIAJ-Style QFP Mid-Temperature Tray for 64LD QFP, 80LD SQFP, and 100LD SQFP

Table A-1. EIAJ-Style QFP High-Temperature Tray

Dimensions	Symbol	64LD QFP	80LD SQFP	100 LD SQFP
Pocket Cntr Location to Edge Y	M	18.5 ±0.1	18.5 ±0.1	18.5 ±0.1
Pocket Cntr Location to Edge X	M1	21.5 ±0.1	21.5 ±0.1	21.5 ±0.1
Pocket-Pocket Cntr Distance X	M2	31 ±0.1	31 ±0.1	31 ±0.1
Pocket-Pocket Cntr Distance Y	M3	32 ±0.1	32 ±0.1	32 ±0.1
Edge Y to Tray Notch	Y1	90	120	120
# of Rows of Pockets	Row Direction as in Drawing	5	5	5
# of Columns of Pockets	Column Direction as in Drawing	8	8	8
Total # of Pockets	Pocket Locations	40	40	40

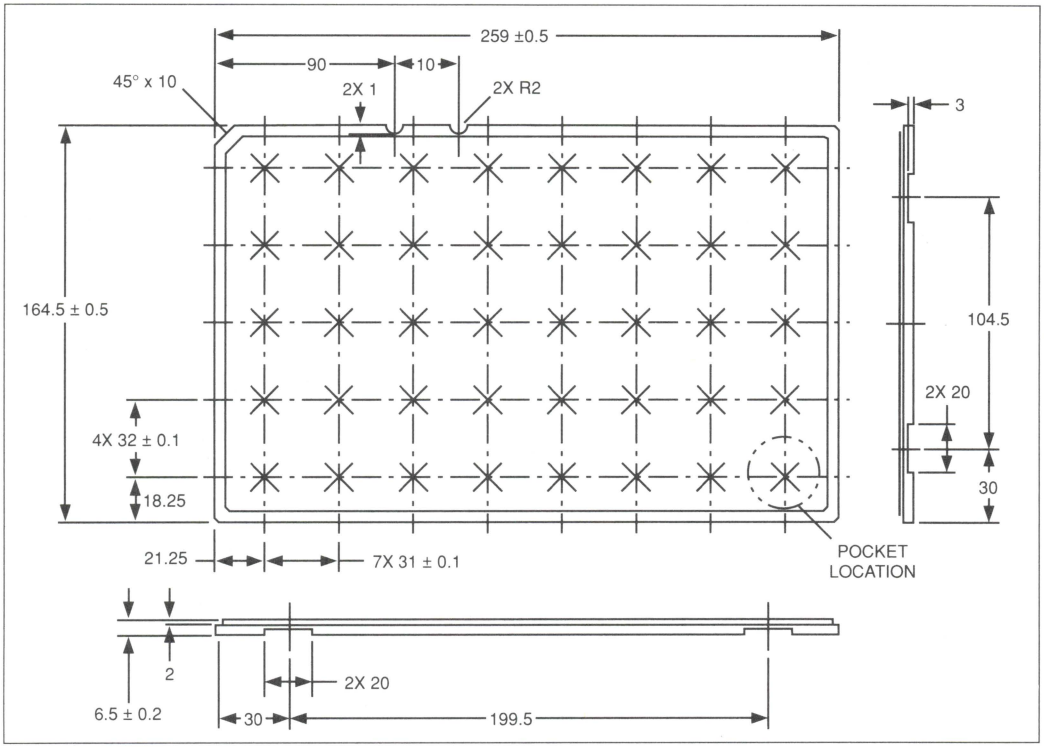


Figure A-3. EIAJ-Style 80/100 Lead (14x20) QFP Mid-Temperature Tray

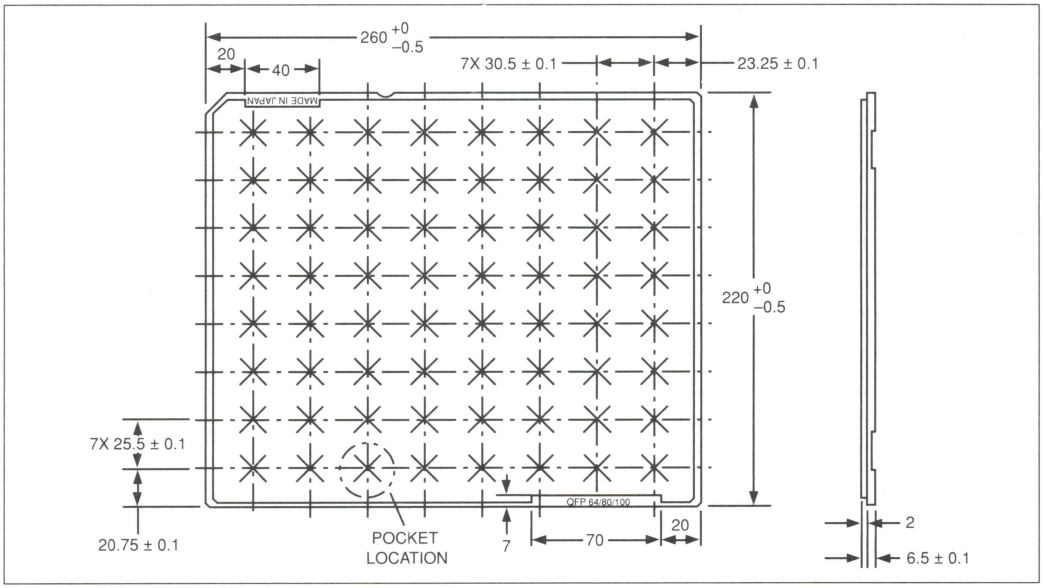


Figure A-4. EIAJ-Style 80/100 Lead QFP (14x20) Low-Temperature Tray

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